Black Book

Edition 7

Higher Speed Ethernet (40GE/100GE)

http://www.ixiacom.com/blackbook

June 2011

Your feedback is welcome

Our goal in the preparation of this Black Book was to create high-value, high-quality content. Your feedback is an important ingredient that will help guide our future books.

If you have any comments regarding how we could improve the quality of this book, or suggestions for topics to be included in future Black Books, contact us at ProductMgmtBooklets@ixiacom.com.

Your feedback is greatly appreciated!

Contents

How to Read this Book

The book is structured as several standalone sections that discuss test methodologies by type. Every section starts by introducing the reader to relevant information from a technology and testing perspective.

Each test case has the following organization structure:

Overview	Provides background information specific to the test case.
Objective	Describes the goal of the test.
Setup	An illustration of the test configuration highlighting the test ports, simulated elements and other details.
Step-by-Step Instructions	Detailed configuration procedures using Ixia test equipment and applications.
Test Variables	A summary of the key test parameters that affect the test's performance and scale. These can be modified to construct other tests.
Results Analysis	Provides the background useful for test result analysis, explaining the metrics and providing examples of expected results.
Troubleshooting and Diagnostics	Provides guidance on how to troubleshoot common issues.
Conclusions	Summarizes the result of the test.

Typographic Conventions

In this document, the following conventions are used to indicate items that are selected or typed by you:

- **Bold** items are those that you select or click on. It is also used to indicate text found on the current GUI screen.
- *Italicized* items are those that you type.

Dear Reader

Ixia's Black Books include a number of IP and wireless test methodologies that will help you become familiar with new technologies and the key testing issues associated with them.

The Black Books can be considered primers on technology and testing. They include test methodologies that can be used to verify device and system functionality and performance. The methodologies are universally applicable to any test equipment. Step by step instructions using Ixia's test platform and applications are used to demonstrate the test methodology.

This seventh edition of the black books includes eighteen volumes covering some key technologies and test methodologies:

Volume 1 – Higher Speed Ethernet

Volume 2 – QoS Validation

Volume 3 – Advanced MPLS

Volume 4 – LTE Evolved Packet Core

Volume 5 – Application Delivery

Volume 6 – Voice over IP

Volume 7 – Converged Data Center

Volume 8 – Test Automation

Volume 9 – Converged Network Adapters

Volume 10 – Carrier Ethernet

Volume 11 – Ethernet Synchronization

Volume 12 – IPv6 Transition Technologies

Volume 13 – Video over IP

Volume 14 – Network Security

Volume 15 – MPLS-TP

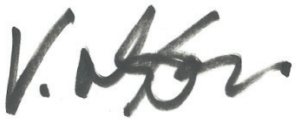
Volume 16 – Ultra Low Latency (ULL) Testing

Volume 17 – Impairments

Volume 18 – LTE Access

A soft copy of each of the chapters of the books and the associated test configurations are available on Ixia's Black Book website at http://www.ixiacom.com/blackbook. Registration is required to access this section of the Web site.

At Ixia, we know that the networking industry is constantly moving; we aim to be your technology partner through these ebbs and flows. We hope this Black Book series provides valuable insight into the evolution of our industry as it applies to test and measurement. Keep testing hard.



Victor Alston, CEO

Higher Speed Ethernet (40GE/100GE)

Test Methodologies for Early Adopters

Network equipment manufacturers and communications chip developers started delivering products in 2010 for the emerging higher speed Ethernet (HSE) market. Carriers, Service Providers, and Large Enterprises are preparing for deployment of 40 and 100-Gigabit Ethernet-based (100 GE) services. There are now public announcements of live, public network demonstrations, white papers published on public interoperability tests through the Ethernet Alliance, and early deployments of 100 GE by Carriers. Server manufacturers are implementing new high performance products with 40 Gigabit Ethernet (40 GE) performance levels and physical interfaces. Web appliances and security devices are capable of operating at 40 GE line rate speed. Globally, there are many companies bringing up new products and services for 40 and 100-Gigabit Ethernet. HSE is driven, in part, by the recent IEEE 802.3ba-2010 standard (802.3ba) that was ratified on June 17, 2010. The ratification was publicly announced on June 21, 2010 and is available at:
http://standards.ieee.org/announcements/2010/ratification8023ba.html
The new standard will be eventually incorporated into the IEEE 802.3-2008 base standard.

Introduction to IEEE 802.3ba-2010 Higher Speed Ethernet for 40 Gb/s and 100 Gb/s

The growth in required Internet bandwidth has been estimated to be anywhere between 75 percent to over 125 percent year over year. Internet growth can be attributed to large increase in the number of broadband access users, increases in the number and complexity of applications that deliver multi-media content, and to the significant growth in wireless users – all combined with the always-on subscriber lifestyle.

In a white paper[1] from the Ethernet Alliance (November 2008):

> "For more than 30 years, Ethernet has evolved to meet the growing demands of packet-switched networks. It has become the unifying technology enabling communications via the Internet and other networks using Internet Protocol (IP). Due to its proven low cost, known reliability, and simplicity, the majority of today's internet traffic starts or ends on an Ethernet connection. This popularity has resulted in a complex eco-system between carrier networks, enterprise networks, and consumers creating a symbiotic relationship between its various parts." (p. 2).

Ethernet is moving into the WAN and is becoming the interface of choice for service providers and carrier data center links, partly due to the efforts of the IEEE 802.3ba-2010 Task Force that defined the new HSE standard for 40 GE and 100 GE Ethernet interfaces. This is the first IEEE 802.3 Ethernet standard that defined two different speeds in one standard. The new standard will expand the use of 10-Gigabit Ethernet (10GbE) drive Ethernet deeper into large Enterprise networks, metropolitan area networks (MAN), wide area networks (WANs) and into data centers – to be utilized by servers and storage networks in the deployment of converged Ethernet data centers.

This test methodology booklet describes the most critical layer 1, sub-layer 2, and layer 2 test areas that new HSE technology adopters are required to test. Ixia's K2 40 and 100 GE test products are layer 1 through 7 capable. They are designed to validate correct operation and compliance to the IEEE 802.3ba-2010 standard by using standard, pluggable port interfaces such as new CFP MSA and QSFP+ SFF-8436.

Early adopters of HSE technology have been using layer 1 and 2 test equipment since the 2H of 2008 and in early 2009. In late 2008 and in the first half of 2009, several HSE test and network products were announced and introduced to the market. In 2010, network

[1] EA Paper – http://www.ethernetalliance.org/files/static_page_files/83AB2F43-C299-B906-8E773A01DD8E3A04/40G_100G_Tech_overview(2).pdf

devices have implemented full layer 2 functionality and an array of layer 3 services that cater to the metropolitan and carrier data centers. This booklet provides insight on the 802.3ba standard and demonstrates layer-2 and sub-layer 2 Ethernet test methodologies that will ensure a product's interoperability and compliance to the standard.

The IEEE 802.3ba standard

Background and Market Drivers

The IEEE was approached in 2006 by several large telecommunications carriers, Internet service providers and financial institutions that provide different Internet services to their internal and external customers. They asked what the IEEE is doing to define standards for transmission speeds higher than 10 Gb/s (that is, IEEE802.3ae and several derivative standards). These companies have several common problems:

1. Supporting high demand for more bandwidth in their data centers.
2. The need for faster data transmissions for electronic business transactions.
3. Simplify networks that use complex link aggregation protocols to increase data throughput.
4. Take advantage of new ultra-high performance servers becoming available to run applications in data centers.
5. Dramatic growth in the number of broadband access subscribers utilizing the latest bandwidth-hungry applications. Figure 1 shows plots the growth in broadband subscribers accessing the Internet.
6. Carriers must continue to lower costs even though IP traffic continues to increase by 50–100 percent each year. New generations of carrier Ethernet switches and Ethernet configured routers will support the achievement of these goals[2].

[2] Machowinski, M., Howard, M. (2010, February), *10G/40G/100G Annual Worldwide Market Size and Forecast*. Roadmap, Drivers, Demand Data, (pg. 1)

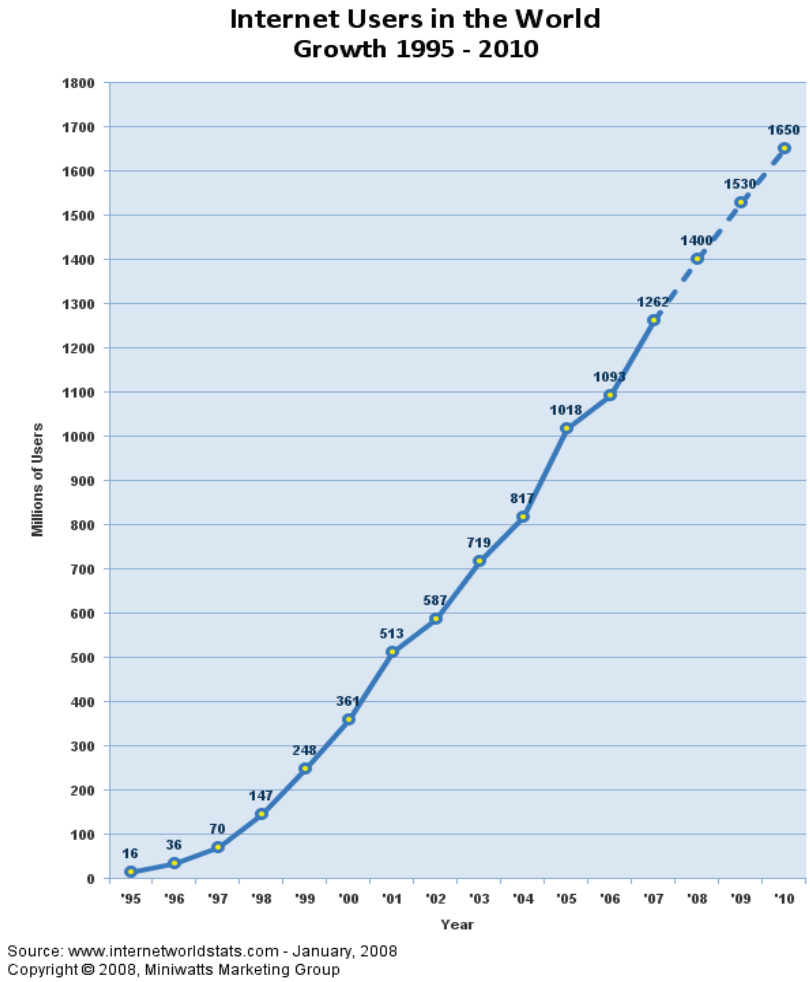


Figure 1. Growth in Internet users (1995–2010)

The forces behind the growth in the use of the Internet shown in Figure 1 are:

- Global Internet data volumes are doubling every 14 months.
- The Internet user population is growing quickly:
  - 90 million were added in China in 2007, alone.
- Service providers are enhancing service offerings:
  - VoIP, VPN, IPTV, peer video, HDTV, video IM, Video on Demand, gaming and online commerce.
- Users are migrating to broadband, causing overload for service providers, data center operators and Internet hubs

- A growing list of industries that are increasing their dependence on the Internet:
    - Education, online commerce, medicine, social networking, security, finance, news, retailing, manufacturing, sports, telecommuting, on and on…

10 Gigabit Ethernet (10 GbE) was introduced by the IEEE in the 802.3ae standard in August 2002. 10 GbE is currently a multiple billion dollar market. As recently reported by Infonetics Research (2009, March)[2], "Annual shipments of 10 Gigabit (10G) and 40 Gigabit (40G) optical carrier and Ethernet ports on enterprise and service provider networking equipment jumped 86% in 2008, nearing 2 million, providing manufacturers $10.8 billion worldwide in 2008, up 45% from 2007."

Although there have been a number of follow-on standards that defined new interfaces and media types for 10 GbE network devices, there had not been an effort to define a higher transmission speed for Ethernet since 2002. 10 GbE Ethernet is a fast growing market. In a recent report from Infonetics Research (March, 2009)[3] Matthias Machowinski, Directing Analyst, Enterprise Voice and Data, reported:

> "Downturn or not, network traffic continues to increase and enterprises are responding by building out their networks. Case in point: the Ethernet switching market, where overall port shipments grew only 2% last year, but 10G port shipments grew 78%. The downturn might temper some of this growth, but the fundamental trend remains, and we expect enterprises to continue making investments in their network cores to avoid congestion."

The high growth in 10 GbE port shipments in 2008 is great news. Many carriers and Internet service providers, however, cannot continue to implement 10 GbE links and servers in a cost effective and manageable way. These companies must reduce the number of physical links in their data centers. The largest companies that have deployed 10 GbE to meet the increase in demand for more bandwidth and to provide more services, have reached a point where the number of 10 GbE links they must support has surpassed their capacity to manage them. Link aggregation methods improved throughput with n number of 10 GbE links. The complexity, however, and the time it takes to debug network issues related to link aggregation techniques is high.

Other technologies, such as 40 G SONET, do provide more bandwidth but are expensive on a per-port basis. They are complex to deploy because a good deal of Ethernet traffic must be switched to SONET – not easy, nor cost effective. SONET requires

[2] http://www.infonetics.com/pr/2009/10g-40g-100g-market-research-highlights.asp

[3] http://www.infonetics.com/pr/2009/10g-40g-100g-market-research-highlights.asp

knowledgeable, skilled network engineers for support. Ethernet, overall, is less expensive than SONET technology and much easier to deploy and maintain.

In response to these market forces, the IEEE 802.3 working group established the high speed study group (HSSG) in 2006. Their objective was to study the market and current and emerging technologies that might meet the criterion needed to launch the development of a new IEEE standard. The HSSG group found that it is possible to build a faster form of Ethernet based largely on the foundation of today's 802.3 standards. The new Ethernet speeds would require a few new, additional mechanisms to run Ethernet at 40 Gb/s and 100 Gb/s speeds. The timeline is shown below:

- Call For Interest (CFI) issued by IEEE 802.3 in July, 2006.
- Higher Speed Study Group (HSSG) formed September, 2006.
- Participation was strong from the beginning of the project:
    - NEMs, carriers, ISPs, VLSI foundries, Internet exchange operators, high performance computing shops, optical component companies, test equipment vendors, and copper component companies.
- HSSG members from the USA, Asia, and Europe participated – a broad international appeal.
- The IEEE procedure calls for the definition of the following for a new standard:
    - Define the Objectives
    - Meet the five criteria
        - Broad market potential
        - Compatibility with other 802 standards
        - Distinct identity
        - Technical feasibility
        - Economic feasibility
- The Project Authorization Request (PAR) for 802.3ba was approved in December, 2007.
- In January of 2008 the IEEE P802.3ba Task Force was authorized to develop 40/100 Gb/s amendments to the base IEEE 802.3 standard.

- To date, the IEEE P802.3ba Task Force has produced several technical drafts that met the timeline shown in Figure 2:
    - Draft 1.0 in October of 2008 became an amendment to the 802.3 specification. This is a key development that makes Higher Speed Ethernet compatible with existing Ethernet.
    - For Draft 2.0 in March, 2009, a high percentage of the technical content has been completed.
    - Draft 3.2 was published on March 24th, 2010Final draft was published on June 22nd, 2010.
- The last technical and editorial changes were made in Draft 3.x versions.
- The IEEE 802.3ba Task Force met its June 2010 schedule for ratification of the standard.

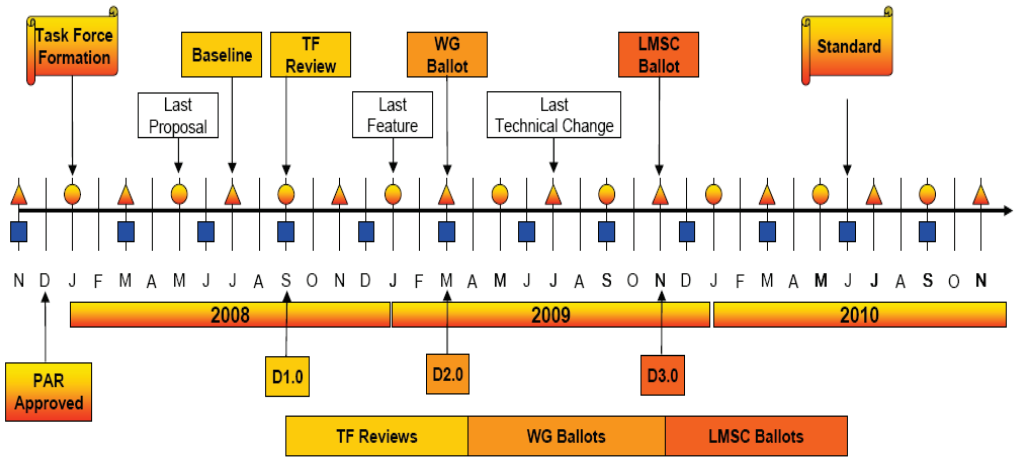


Figure 2. Development timeline for the IEEE P802.3ba standard

Many of the major network equipment manufacturers (NEMs) started product development programs even before Draft 1.0 of the draft standard was published. With the publication of Draft 2.0 in March of 2009, NEMs around the globe were preparing to introduce early products in order to enter into beta with their customers in the second-half of 2009. This is possible because over 90% of the technical content has been defined in draft 2.0. This lowers the risk for the product development teams since changes to the Draft 3.x versions turned out to be minor (in comparison to previous drafts) and did not affect the major, new mechanisms that define 40 Gb/s and 100 Gb/s products. Dozens of companies around the world have 40 Gb/s and 100 Gb/s product development programs running full speed ahead.

Ixia has been involved with the development of the HSE standard since the formation of the HSSG. Ixia has three voting members that worked on the standard. Ixia's major contribution to the development of the standard has been to prototype various mechanisms proposed for the new physical coding sublayer (PCS). The PCS is a key enabler that allows the use of today's component technology to create cost effective products that operate at 40 Gb/s and 100 Gb/s speeds. Ixia prototyped several proposals and presented their finding in 2008 to the IEEE Task Force. Of the various mechanisms that were evaluated, Ixia recommended to the task force a new PCS mechanism known as Multi-Lane distribution (MLD). In the ratified standard, MLD is used to refer to the encoding and PCS Lanes is the terminology used for the logical lanes mechanism. The task force adopted Ixia's recommendation and made it part of the draft standard at the time.

As an example of Ixia's technical leadership, in June of 2008 Ixia publicly demonstrated a working 100 GE proof of concept system that successfully sent and received traffic in a live WAN between Las Vegas and Los Angeles. The 100 GE proof of concept system used a 100 GE MAC built by Ixia that generated 10 lanes of 10Gb/s network traffic per lane over multimode fiber, using an 850 nm wavelength. That data was sent to a digital optical transport network device that switched the Ixia 100 Gb/s aggregate traffic over a combination of DWDM and Digital Optical Network connections. These connections sent the 100 GE traffic to a service provider who routed it back through the optical transport switches, back to the Ixia 100 GE proof of concept system. This demonstration, held at the NXTComm tradeshow in Las Vegas, Nevada, was the world's first public demonstration that used the new MLD PCS (that is, PCS Lanes) mechanism. The demonstration proved that today's component technology can be used to build an Ethernet network in which 10 lanes of 10 Gb/s are aggregated and processed by a 100 Gb/s MAC (Media Access Control protocol per the IEEE 802.3 standard).

In September of 2008 Ixia introduced the world's first 100 GE layer 1 and 2 data communications test system, shown in Figure 3. A 40 Gb/s test system was publicly shown in September, 2008 at the Broadband World Forum in Brussels, Belgium. At that time the test systems conformed to technical Draft 1.0. Because of its FGPA-based design, Ixia was able to rapidly adapt its 40 Gb/s and 100 Gb/s test systems to the changes in technical Draft 2.0 through to the ratification of the final standard in June 2010.

In December of 2008 Ixia sold and delivered the world's first 100 Gb/s IP Ethernet test system to a major NEM. It was called the 100 GE Development Accelerator System. This system was the first time in the IEEE's history of Ethernet that a draft compliant IP test system was commercially available during the development of a draft standard. This system allowed the earliest adopters of HSE technology around the world to make tangible progress in their development programs. This test system used a SNAP12 optical

transceiver interface that delivered full line rate 100 GE Ethernet traffic with a wide array of layer 2 and new physical coding sublayer (PCS) PCS Lanes measurement capabilities.

Figure 3. World's first 100 GE IP Ethernet test and measurement system

Through the first three calendar quarters of 2009, Ixia delivered additional 40 GE and 100 GE SNAP12-based test systems. Ixia was the only test and measurement vendor to deliver production-ready HSE 100 GE and 40 GE test systems into its customer's product development and test environments. All of these systems maintained compliance with the drafts D2.0, D 2.1 and D2.2 of the IEEE P802.3ba draft standard because of their FPGA-based design and Ixia's high degree in-house development of intellectual property. This allowed Ixia to lead the test industry in delivering 40 GE and 100 GE test systems.

During 2009, optical transceiver manufacturers produced a multi-source agreement (MSA) specification for a new type of pluggable transceiver known as CFP. The specification is public and can be found at http://www.cfp-msa.org/index.html. Currently, the major optical transceiver manufacturers are delivering CFP MSA complaint products to network equipment manufacturers, test companies, service providers, and carriers.

The CFP MSA is the current industry standard optical transceiver format for 40 GE and 100 GE hot-pluggable optical transceivers for both multimode fiber up to 100 meters reach range for OM3 fiber and up to 150 meters for OM4 fiber. Single mode fiber has been publicly tested up to 10 kilometer reach range as shown in the following figure. Today, CFP MSA-based optical transceivers are in development for the 40 kilometer reach range as defined by the IEEE802.3ba standard. The multimode CFP transceivers use the MT/MPO connector/cable system and 12-fiber, fiber optic cable for 40 Gbps speed and the 24-fiber, fiber optic cable for 100 Gb/s speed. For single mode fiber, the IEEE 802.3ba and the CFP MSA defined a wavelength-division-multiplexed optical configurations that uses a single transmit and a single receive fiber to carry four wavelengths, with each wavelength operating at a rate of 25.78125 Gbps. This is commonly called a 4 x 25 Gbps configuration.

Overall, the support for multimode and single mode configuration in the CFP MSA makes it the most flexible optical transceiver available.

Figure 4. CFP MSA optical transceiver

Source: REFLEXPHTONICS at:

http://www.reflexphotonics.com/products_0.html#Interboard

However, HSE technology application demands have spawned additional transceiver formats. A new transceiver format known as CXP is emerging as the new format for HSE applications that has a much smaller physical footprint than CFP. The CXP is targeted for high density 100 GE and Infiniband QDR applications that can deliver up to 120 Gbps as shown in the following figure. CXP is being standardized by the Infiniband Trade Accociation.

Figure 5. CXP 120 Gbps active optical cable

Source: MergeOptics at

http://x40msa.com/

QSFP+ SFF-8436 (SFF Committee QSFP document) specification, for example, will serve the short reach, multimode fiber market that has been widely adopted by switch and server manufacturers for data center applications centered around 40 Gb/s speeds. QSFP+ transceiver and cable assembly technology supports up to 100 meter reach range with standard MMF cable products (custom engineered cables may provide

longer lengths). Variants of the QSFP+ specification have produced QSFP+ transceivers that support single mode fiber and can reach up to 10 kilometers reach range while still maintaining electrical and mechanical compliance with the SFF 8439 QSFP+ specification.

Today, there are both Active Optical Cables (AOC) for QSFP+ and both passive and active copper cables assemblies that support QSFP+.

Through the calendar year of 2009, Ixia built an HSE product line based on the CFP MSA optical transceiver format.

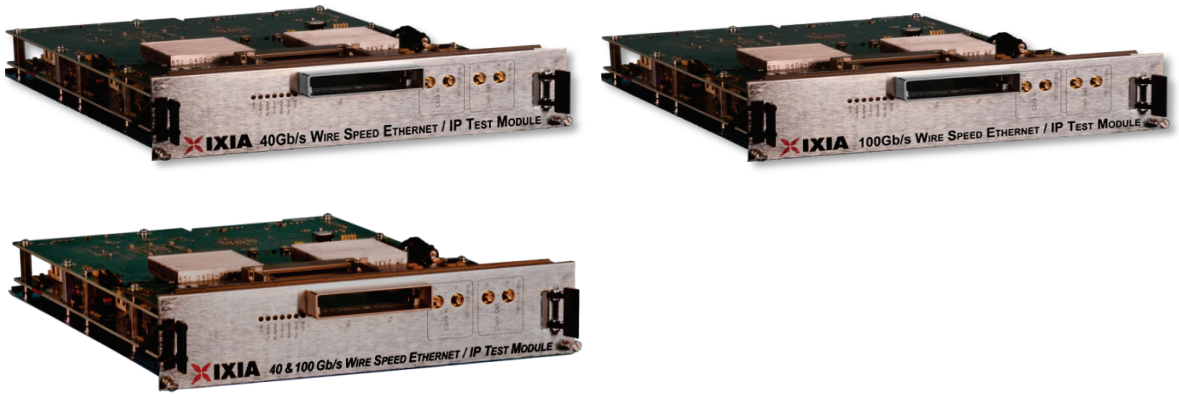


Figure 6. Ixia's 40 Gb/s, 100 Gb/s, and dual speed 40 and 100 Gb/s CFP MSA test interfaces

A picture of Ixia's 40 Gb/s, 100Gb/s and dual speed 40/100Gb/s CFP-MSA test systems is shown above. A technical datasheet on Ixia CFP-based products is available at http://www.ixiacom.com/products/higher_speed_ethernet_testing/index.php .

From the beginning of Ixia's HSE product development there was and continues to be a single platform approach that protects Ixia's customer's investment in HSE test products. The early installations 40 GE and 100 GE SNAP12-based products have all been upgraded to a CFP MSA test systems. A 40 GE or a 100 GE single speed system can be upgrade to become a dual speed 40 GE and 100 GE test system. Ixia is the only test vendor in the industry that can deliver products that supports both of these optical transceiver standards in their native formats.

In June 2010, Ixia introduced a third load module type with pluggable QSFP+ optical transceiver format called QSFP+, shown in Figure 5. Today, QSFP+ is a 40 Gb/s technology. It typically deployed with active optical cable assemblies and passive copper cable assemblies and today, on the market there are the QSFP+ pluggable transceivers that use the MT/MPO connector with a 12-fiber, fiber optic cable for multimode and a duplex 10Gb/s rated fiber cable for single mode applications.

Figure 7. 40 Gb/s QSFP IP test load module

Figure 8. QSFP pluggable transceiver

Source: MergeOptics at

http://x40msa.com/

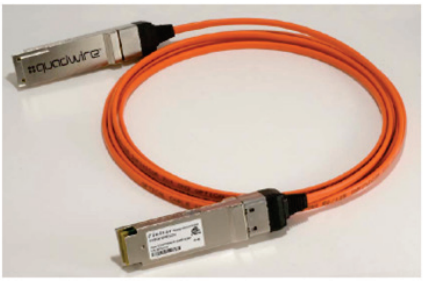


Figure 9. QSFP active optical cable

Source: Finisar Corporation

http://www.finisar.com/product_Quadwire_120

Figure 10. QSFP passive copper cable

Source: Amphenol Cables on Demand at

http://www.cablesondemand.com/category/QSFP%20CBL/product/SF-QSFP2EPASS/URvars/Items/Library/InfoManage/.htm

New HSE network products will find their way into data centers, large carrier and service provider networks, Internet Service Providers and into high-performance servers and computing clusters.

Key Elements of the IEEE802.3ba Standard

Two speeds have been defined: 40 Gb/s and 100 Gb/s. Throughout Ethernet's history, its speed has always increased in steps that multiplied the previous speed by ten: 10 Mbps to 100Mbps, 100Mbps to 1000 Mbps, and 1000 Mbps to 10,000 Mbps. Two questions that are often asked by those new to the HSE ecosystem are:

- Why didn't the standard just follow the history of Ethernet and just define 100,000 Mbps (i.e. 100 Gb/s)?
- Why were two speeds defined for the first time in Ethernet history?

While the HSSG worked to meet the five IEEE criteria to document the justifications for a new HSE standard, it became apparent that the evolution of the technology required for core networks and in large data centers required 100 Gb/s speed. At the same time, manufacturers of computer networking devices (servers, NICs, storage network equipment, high performance servers and computing clusters, and enterprise switches) made a supportable case to the HSSG that these types of computing-application-based network devices will not have the technology available at a reasonable cost and in the same timelines as 100 Gb/s. Computer-based networking devices cannot handle network traffic at 100 Gb/s speeds using today's component technology. Yet,

at the same time, these computer application-based networking devices have great demand for more bandwidth as well.

The IEEE P802.3ba Task Force accommodated these requirements by adding the 40 Gb/s speed to the standard. This strengthened the case for meeting the criteria for a new standard to have broad market potential.

In summary, the standard defines two distinct applications:

- 100 Gb/s for core networking applications
- 40 Gb/s for computer networking devices, computing clusters and storage networks.

One of the main objectives of the HSE standard was to be as compatible as possible with existing Ethernet technologies.

The primary objectives for the new standard are shown below:

Support full-duplex operation only.

- Preserve the 802.3 Ethernet frame format utilizing the 802.3 MAC.
- Preserve minimum and maximum frame size of current 802.3 standard.
- Support a bit error rate (BER) > to 10^{-12} at the MAC/PLS service interface.
- Provide appropriate support for Optical Transport Networks (OTN).
- Support a MAC data rate of 40 Gb/s.
- Provide physical layer specifications which support 40 Gb/s operation over:
    - At least 10km on single mode fiber (SMF).
    - At least 100m on OM3 multi mode fiber (MMF).
    - At least 7m over a copper cable assembly; this was originally 10 meters
    - At least 1m over a backplane.
- Support a MAC data rate of 100 Gb/s using the existing 802.3 protocol.
- Provide physical layer specifications which support 100 Gb/s over:
    - At least 40km on SMF.
    - At least 10km on SMF.
    - At least 100m on OM3 MMF.

- At least 7m over a copper cable assembly; this was originally 10 meters

These objectives are supported by numerous compatibilities to existing 802.3 and 802.1 standards that make the new HSE easier to integrate with existing Ethernet network devices and networks. This increases compatibility with the installed base of Ethernet equipment from the perspective that it will be relatively easy to pass 1GbE and 10 GbE traffic into switch fabrics that can forward at the higher 40 Gb/s and 100 Gb/s rates. To take this a bit further, with support for optical transport networks (OTNs), 40 Gb/s and 100 Gb/s traffic can ingress to an optical switch that allows 40 Gb/s and 100 Gb/s sourced traffic to be forwarded by OTN optical switches that are connected to MAN and WAN core optical networks.

New optical transceivers and copper cables have been developed for the HSE standard to support the media described in Tables 1 and 2 below.

Table 1. Media types for Higher Speed Ethernet

	40 Gigabit Ethernet	100 Gigabit Ethernet
At least 1 meter backplane	√	
At least 7 meter copper cable	√	√
At least 100 meter OMC MMF fiber	√	√
At least 10km SMF	√	√
At least 40km MMF		√

Source: Ethernet Alliance (2008, November), 40 Gigabit Ethernet and 100 Gigabit Ethernet Technology Overview, p3. http://www.ethernetalliance.org/files/static_page_files/83AB2F43-C299-B906-8E773A01DD8E3A04/40G_100G_Tech_overview(2).pdf. Edited on September, 2009 for compliance with the D2.2 standard.

Table 2. Media types and nomenclature for 40 Gb/s and 100 Gb/s per IEEE P803.3ba

	40 Gigabit Ethernet	100 Gigabit Ethernet
At least 1 meter backplane	40GBASE-KR4	
At least 7 meter copper cable	40GBASE-CR4	100GBASE-CR10
At least 100 meter OMC MMF fiber	40GBASE-SR4	100GBASE-SR10
At least 10km SMF	40GBASE-LR4	100GBASE-LR4
At least 40km MMF		100GBASE-ER4

Source: Ethernet Alliance (2008, November), 40 Gigabit Ethernet and 100 Gigabit Ethernet Technology Overview, p10. http://www.ethernetalliance.org/files/static_page_files/83AB2F43-C299-B906-8E773A01DD8E3A04/40G_100G_Tech_overview(2).pdf. Edited on September 2009 for compliance with the D2.2 standard.

The task force included a broad set of components and subsystems in the standard that have not been included in past Ethernet standards. Backplanes and copper media were added to the standard along with fiber media.

The following figure shows the new HSE Layer model.

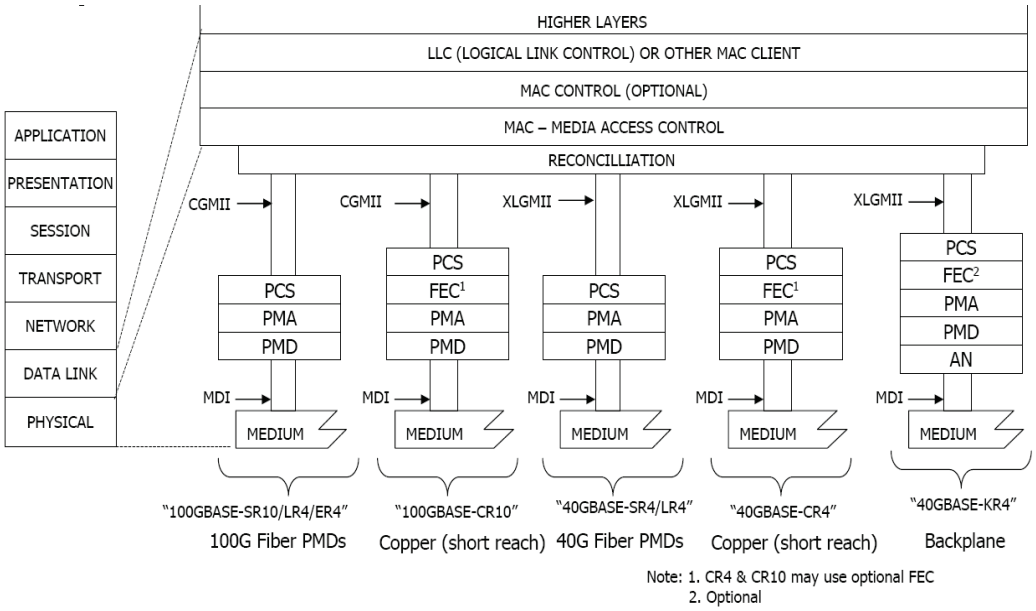


Figure 11. The new IEEE802.3ba physical layer model

This has necessitated a new nomenclature for the different families of HSE systems. The following figure shows a summary table from the standard with these definitions.

- **Rate**
  - 40=40Gbps, 100=100Gbps
- **Medium**
  - Copper
    - K=Backplane
    - C=Cable assembly
  - Optical
    - S=Short Reach (100m)
    - L=Long Reach (10km
    - E=Extended Reach (40km)
- **Coding Scheme**
  - 64B/66B block encoding
- **Number of Lanes or Wavelengths**
  - Copper: 4 or 10
  - Optical: 4 or 10
  - Serial optical: 1

PHY description	Port Type
40G Backplane PHY	40GBASE-KR4
40G Cable Assembly PHY 100G Cable Assembly PHY	40GBASE-CR4 100GBASE-CR10
40G MMF 100m PHY (Ribbon) 100G MMF 100m PHY (Ribbon)	40GBASE-SR4 100GBASE-SR10
40G SMF 10Km PHY 100G SMF 10Km PHY	40GBASE-LR4 100GBASE-LR4
100G SMF 40Km PHY	100GBASE-ER4

Figure 12. IEEE P802.3ba physical layer nomenclatures

Difference between 10 GbE and Higher Speed Ethernet

The key differences between 10 GbE technology and mechanisms compared to 40 Gb/s and 100 Gb/s are:

1. 10 GbE uses serial media: one fiber for optical implementations supported by a PCS that runs at 3.125 Gbps over each of 4 lanes (XAUI) that are combined into a single serial stream over the fiber.

   Some 10 GbE technologies do use multiple copper lanes. These include 10GBASE-CX4 and those technologies that use multiple wavelengths, such as 10GBASE-LX4, that are managed by a fixed PCS mechanism called XAUI. XAUI uses multiple lanes or wavelengths feeding into a 10 Gb/s MAC. Regardless of how a 10 GbE system is configured there is no additional traffic throughput: it is still 10 Gb/s.

   40 Gb/s and 100 Gb/s use parallel electrical lanes with multiple fiber optical media. The 40 Gb/s PCS runs at 10.3125 Gbps over each of 4 physical lanes combining for 40 Gb/s. The 100 Gb/s PCS uses 10 physical lanes of 10 Gb/s each, combining for 100 Gb/s. The parallel, higher speed per lane schema used in HSE, transmitters and receivers required a new, more flexible PCS mechanism (that is, MLD for encoding and PCS Lanes for logical lanes support). For single mode 10 kilometer and 40 kilometer reach ranges, there are four wavelengths running over one fiber at 10.3123 Gbps each for 40 Gb/s and for 100 Gb/s these four wavelengths each run at 25.78125 Gbps. There is no current component technology that can operate at serial 40 and 100 Gb/s in the 2010 through 2012 timeframe. In order to meet the market demand for higher speed Ethernet a new PCS mechanism (that is, MLD and PCS Lanes) became a requirement.

2. The new HSE PCS mechanism uses a lane identification marker and has periodic synchronization in order to maintain lock. Such a mechanism does not exist in the same way at 10 GbE. In 10 GbE XAUI, lanes are always mapped as lane 0, 1, 2 and 3 in round robin fashion. 10 GbE always aligns the lanes relative to lane 0 with a single alignment character that aligns across all lanes.

   With 40 and 100 Gb/s, the lanes mechanism allows the 64B/66B encoded blocks to travel over any of the multiple lanes. The lanes align themselves in specific time frames to the first synchronized lane.

The MAC, however, works in the same manner at 10 Gb/s, 40 Gb/s and at 100 Gb/s. This increases the compatibility of various Ethernet speeds and is one of several elements that make it easier to build HSE components that can switch from one speed to

another. 10, 40 and 100 GbE use the same 64B/66B encoded blocks (also called encoded words or payloads).

Physical Coding Sublayer for Higher Speed Ethernet

Since the physical coding sublayer is one of the HSE critical enablers. It is important to become familiar with it in order to learn how to test it. The operation of the new PCS lanes mechanism is integral to bringing up a layer-2 network device with a solid link.

The figures below are extracted and paraphrased from Ixia's white paper (2008, June), *Enabling 100 Gigabit Ethernet Implementing Multilane Distribution in the PCS Layer*, p3.[4]

The IEEE 802.3 Protocol Stack

The following figure shows a simplified version of the IEEE 802.3 protocol stack as it relates to the PCS layer and the unique requirements for 40 Gb/s and 100 Gb/s Ethernet.

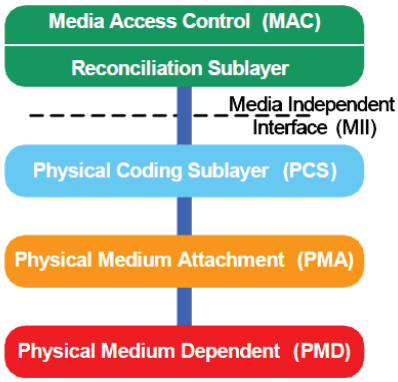


Figure 13. IEEE802.3ba physical layer nomenclature

The simplified version of an 802.3 stack is translated in the next section into an example of what a 100 Gb/s HSE link looks like in terms of the architecture in the 802.3ba standard.

100 Gb/s and 40 Gb/s link architecture and optical transceivers

Figure 13 shows the architectural partition for a 100 Gb/s Ethernet link. The partitioning assumes:

1. A highly integrated 100 Gb/s MAC/PCS chip that includes the packet interface and MAC, PCS, and PMA functions.

[4] http://www.ixiacom.com/pdfs/library/white_papers/PCS_white_paper.pdf

2. An optical module that includes both PMA and PMD functions.
3. A high-speed parallel electrical interface comprising ***n*** lanes between the MAC/PCS chip and the optical module.
4. A parallel optical interface comprising ***m*** lanes, where lanes can be wavelengths or fibers.

If we zoom in on Figure 14's simplified link, we can review an example architecture of a 100 Gb/s optical transceiver design (in the blue box in the figure) relative to the 802.3ba standard and the PCS Lanes Mechanism.

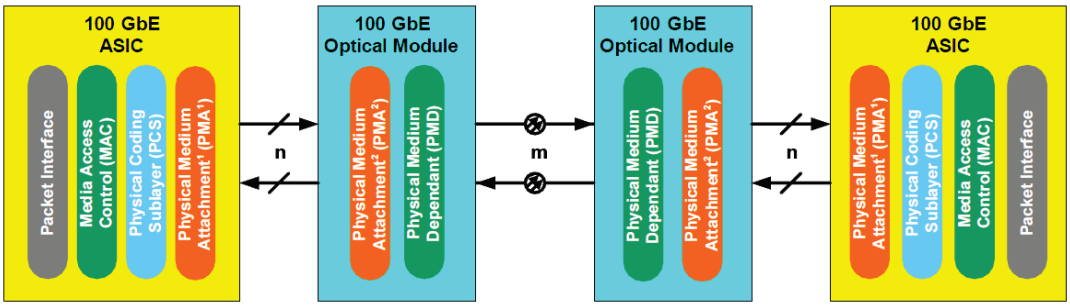


Figure 14. Architectural partitions for a 100 Gb/s link

Figure 15 is a 4 by 25 Gb/s single mode fiber (SMF) 10 km reach range PMD architecture example. The 10 electrical lanes running at 10 Gb/s are serialized and multiplexed inside the transceiver to four lanes (in this case, four different wavelengths) running at 25.78125 Gbps for transmission and reception using optical WDM technology over SMF (the ***m*** lanes in 14). In Figure 14, the ***n*** lanes are the 10 physical electrical lanes on the transmit side and the 10 physical electrical lanes on the receive side.

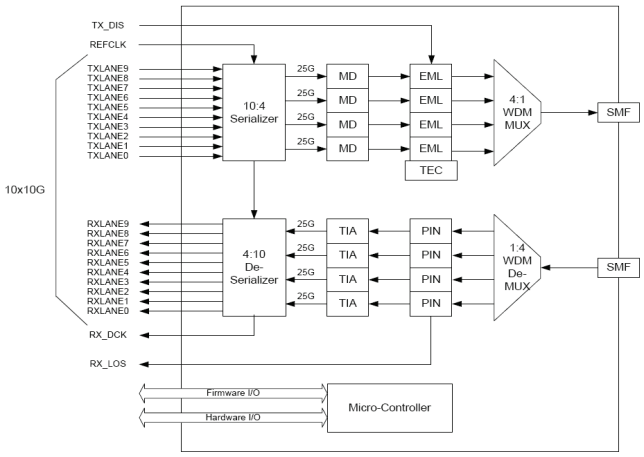


Figure 15. PMD architecture for a 4 x 25 Gb/s 10 Km PMD (transceiver)

Source: IEEE 802.3ba meeting on May 14, 2008, in Munich. Germany

The PCS mechanism does not change in this 100 Gb/s transceiver example because the serialization/multiplexing on the transmit side and de-serialization/de-multiplexing on the receive side take place inside the optical transceiver. The PCS mechanism services the 10 transmit and 10 receive lanes. The PCS mechanism does not care what the optical transceivers do with respect to its configuration of the encoded blocks and lane alignment markers as long as the optical transceivers maintain the correct timing synchronization, and deliver the data intact, and at the required speed for the PCS mechanism to maintain synchronization for the link. All the optical transceivers in the standard source their reference clock from the device that they are installed into.

There is an architectural separation between the transmit and receive sides of the PCS mechanisms versus the optical transceivers. The receiving PCS mechanism has the challenging job of re-combining the PCS Lanes data delivered by the optical transciever. The optical transceiver can send PCS data in any order and the receive side must be able to recombine it correctly while maintaining synchronization.

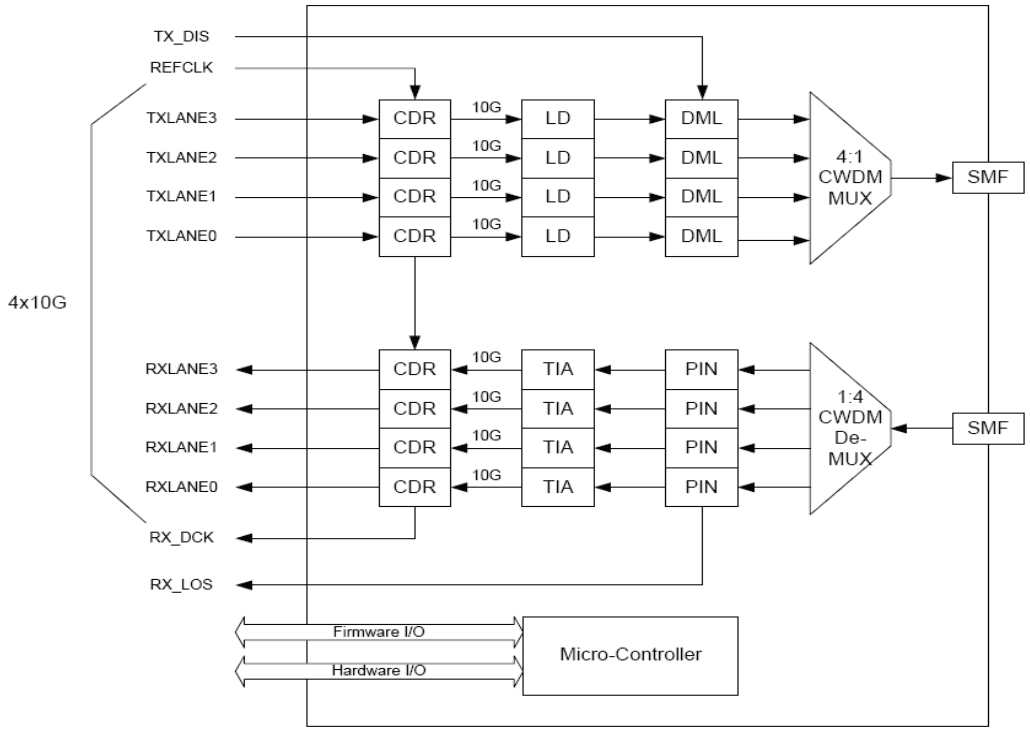


Figure 16. PMD architecture for a 4 x 10 Gb/s 10 Km PMD (transceiver)

Source: IEEE 802.3ba meeting on May 14, 2008, in Munich. Germany

Figure 16 represents an example of a 40 Gb/s optical transceiver architecture for single mode fiber with a CWDM delivery configuration. There are 4 physical electrical lanes on the transmit-side and 4 physical electrical lanes on the receive-side; each lane carries 10.3125 Gbps. The PCS mechanism follows the same rules as described for the 100 Gb/s PMD CWDM system in Figure 15.

PCS Mechanism with MLD Design

As shown in Figure 15, the PCS translates between the respective media independent interface (MII), shown in Figure 13, for each rate (40 Gb/s and 100 Gb/s) and the PMA sublayer. The PCS is responsible for the encoding of data bits into code groups for transmission via the PMA and the subsequent decoding of these code groups from the PMA.

The task force developed a low overhead scheme, referred to as multilane distribution (MLD), as the basis for the PCS for 40 and 100 Gb/s Ethernet.

The PCS MLD scheme has been designed to support all PHY types for both 40 and 100 Gb/s Ethernet. It is flexible and scalable. Furthermore, the PCS will support future PHY types that may be developed that will be fueled by continuous advances in electrical and optical transmission. The PCS layer also performs the following functions:

- Frame delineation.
- Transportation of control signals.
- Ensure necessary clock transition density as needed by the physical optical and electrical technology.
- Stripe and re-assemble the information across multiple lanes.

The PCS Lanes leverages the 64B/66B coding scheme that was used in 10 Gb/s Ethernet. It provides a number of useful properties, including low overhead and sufficient code space to support necessary code words, which are also consistent with 10 Gigabit Ethernet.

The MLD scheme implemented in the PCS Lanes is fundamentally based on a striping of the 66-bit blocks across multiple lanes. The mapping of the lanes to the physical electrical and optical channels that will be used in any implementation is complicated by the fact that the two sets of interfaces are not necessarily coupled. Technology development in either chip interfaces or optical interface is not always tied together, and it was necessary to develop the concept of PCS lanes to allow the decoupling of the evolution of the optical interface widths from the evolution of the electrical interface widths.

The transmit PCS, therefore, performs the initial 64B/66B encoding and scrambling on the aggregate channel (40 or 100 Gb/s) before distributing 66-bit block in a round robin basis across the PCS lanes, as illustrated in Figure 17.

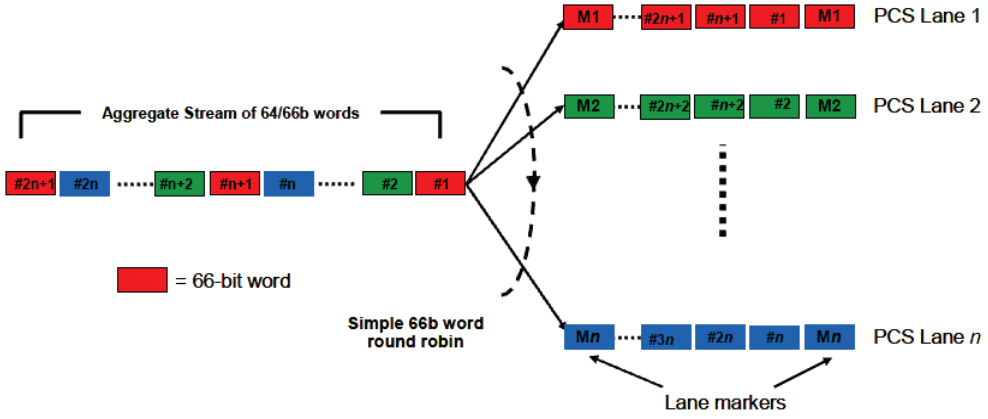


Figure 17. PCS Lane distribution concept

The number of PCS lanes needed is the least common multiple of the expected optical and electrical interfaces widths. For 100 Gb/s Ethernet, 20 PCS lanes are used. The number of electrical or optical interface widths supportable in this architecture is equivalent to the number of factors of the total PCS lanes. Therefore, 20 PCS lanes support interface widths of 1, 2, 4, 5, 10 and 20 channels or wavelengths. For 40 Gb/s Ethernet 4 PCS lanes support interface widths of 1, 2, and 4 channels or wavelengths.

Once the PCS lanes are created, they can then be multiplexed into any of the supportable interface widths. Each PCS lane has a unique lane marker, which is periodically inserted. All multiplexing is done at the bit-level. The round-robin bit-level multiplexing can result in multiple PCS lanes being multiplexed into the same physical channel. The unique property of the PCS lanes is that no matter how they are multiplexed together, all bits from the same PCS lane follow the same physical path, regardless of the width of the physical interface. This enables the receiver to be able to correctly re-assemble the aggregate channel by first demultiplexing the bits to re-assemble the PCS lane and then re-align the PCS lanes to compensate for any skew. The unique lane marker also enables the deskew operation in the receiver. Bandwidth for these lane markers is created by periodically deleting inter-packet gaps (IPG). These alignment blocks are also shown in Figure 17.

The receiver PCS sees all these multiple PCS lanes, realigns them using the embedded lane markers and then re-orders the lanes into their original order to reconstruct the aggregate signal.

Two key advantages of the MLD and PCS Lanes methodology are that all the encoding, scrambling and deskew functions can all be implemented in a CMOS

device, which is expected to reside on the host device, and minimal processing of the data bits other than bit-muxing happens in the high speed electronics embedded with an optical module. This simplifies the functionality and ultimately lowers the costs of these high-speed optical interfaces.

Layer 2 Ethernet Test Methodologies

Testing layer 1-3 Ethernet network devices can require a complex and extensive set of tests. This test methodology booklet specifically addresses critical layer-2 and sub-layer 2 functional tests that early adopter product development teams will require to validate their compliance of early electronics hardware and software.

The test challenges addressed by early adopter teams revolve around technical feasibility studies, simulations, product prototyping, algorithm development verification, system timing quantification and error-debugging.

Typical test challenges for new hardware and design validation for early HSE adopters are:

- Bringing hardware electronics assemblies up to a functional state with which to generate and receive encapsulated Ethernet traffic.
- Validating the new PCS lane operation.
- Integrating firmware and software with hardware electronics assemblies.
- Integration of optical and copper transceivers to hardware electronics assemblies.
- Verification of an entire network device system operating at line rate for all supported packet sizes and rates.
- Stress testing at layer 2 that includes transmit and receive compliance, including negative tests.
- Interoperability with other manufacturer's HSE network devices.
- Validation the compliance to the IEEE 802.3ba standard.

Several test areas are critical in the early stages of electronics hardware development programs for a number of devices:

- Applications-specific integrated circuit (ASIC)
- Field programmable gate array (FPGA)
- System on a chip (SOC): a form of ASIC
- Integration of chips and memory devices on printed circuit board assemblies (PCBA) that eventually become switch blades or switching fabrics

Product development teams must make efforts to ensure standards-compliance so that they can integrate with other components and systems in the future.

This version of the HSE test methodology booklet focus on two critical use cases for that hardware and firmware developers face when their 40 and 100 Gb/s PCBAs becomes operational.

Physical Coding Sublayer for Higher Speed Ethernet Technology

There are several reasons for building a new physical coding sublayer (PCS) for 40 100 Gb/s:

1. There are currently no commercially available devices that can operate at serial 40 Gb/s and 100 Gb/s rates over existing media.
2. The development of electrical interfaces to support 40Gb/s and 100 Gb/s rates are not necessarily coupled to the development of fiber and copper media devices that can support these higher Ethernet rates.
3. Network equipment manufacturers are highly cost sensitive. Therefore, component cost and immediate high-volume availability become primary drivers. NEMs need a flexible way to implement HSE network devices and media that are practical to implement and cost effective.

There was a need to have greater flexibility than the 10 GbE PCS mechanism that allows the use of readily available communications device components that operate at 10Gb/s. This allows 40 Gb/s and 100 Gb/s to be spread out over a number of 10Gb/s lanes which are recombined and aggregated to produce Ethernet links with media that can handle 40 Gb/s and 100 Gb/s speeds.

Validation of the Physical Coding Sublayer

Ixia's IxExplorer 40 and 100 Gb/s functionality addresses both receive-side and transmit-side elements of PCS lane functionality, including data, alignment and control payloads:

Receive-side testing

The major considerations for receive side testing are:

- 64B/66B sync bit lock
- PCS lane alignment marker lock
- Skew tolerance and compensation

- Arbitrary mapping of received to transmitted PCS lanes
- Detection of sync errors in alignment lane markers
- Detection of lane marker errors
- Detection of BIP errors
- Detection of sync and [payload errors injected into in 64/66 bit encoded words

Transmit-Side Testing

The major considerations for the transmit-side testing are the verification and monitoring of various attributes:

- 64B/66B encoded blocks and sync bits. Proper transmission of encoded blocks and their sync bits must be determined and then monitored. Detection and counting of erroneously encoded blocks and their sync bits must be available in real-time.
- PCS lane alignment markers. Proper transmission of alignment markers must be verified and monitored, with real-time error counts.
- Lane skew insertion adds a known value of time delay to one or more PCS lanes that must be measured.
- Sync field bit error injection
- Alignment Lane Marker error injection
- BIP3 and BIP7 error injection
- 64/66 bit encoded word error injection

PCS Layer Test Objectives

The test objectives for the 40 and 100 Gb/s PCS layer are:

1. Lane mapping – validate correct transmit lane and receive mapping operations under a range of different transmit mapping skew conditions and configurations.
2. Lane skew measurements – directly measure PCS lane skew on the receive port while deliberately injecting lane skew at the transmit port in order to stress test the device under test (DUT). This can be used to validate the compliance of the PCS lane skew to the IEEE 802.3ba standard's maximum tolerance. This capability may be used to perform negative, stress and range tests.
3. 64B/66B encoded block synchronization required to maintain a HSE link.

4. PCS lane synchronization and lane marker alignment – validate that 64B/66B encoded blocks achieve bit-synchronization, verify that the virtual lane is associated with the correct physical lane. Determine if alignment markers have locked with their physical lane.

5. Detect and count PCS errors and PCS lane alignment errors in real time.

6. PCS lane mapping. The actual mapping of transmitted to received PCS lanes must be identified and reported for verification.

Getting Started with PCS Lane Testing

Physical Test Topology for PCS Layer test methodology

Ixia's 100 Gb/s load module using a SNAP12 transceiver and multimode fiber ribbon cable is used for all of the PCS lane test methodologies.

This allows a demonstration of the principles of Ixia's PCS layer test system. The Tx and Rx sides of this one port load module are separate multi-push-on (MPO) connectors. The system uses 10 fibers of the 12-fiber ribbon cable (SNAP12) to distribute 10 separate lanes of 10 Gb/s traffic. Each fiber uses the same 850 nm multimode wavelength with OM3 fiber media. This configuration produces an aggregate of 100 Gb/s. The Ixia MAC runs at full line rate of 100Gbps on both transmit and receive ports.

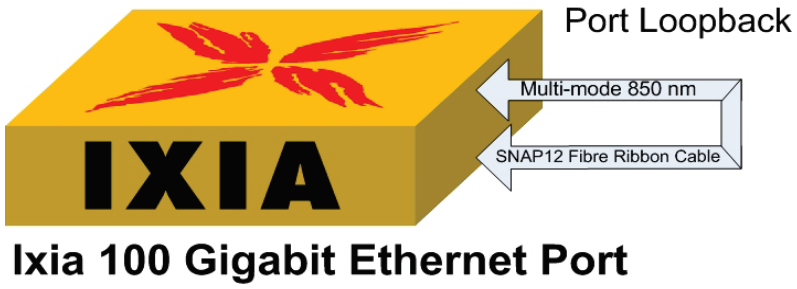


Figure 18. Ixia 100 Gb/s test system in loopback

Two GUI screens have been added to Ixia's IxExplorer test software for HSE. These screens provide the ability to simply configure the Tx port and measure PCS lane properties on the Rx side. All PCS lane tests execute in real time and are integral with the establishment of link. The moment a cable is plugged in between two end points, or immediately after a Tx configuration is applied, measurements commence. The Rx screen link status and measurements are automatically determined by Ixia's IxExplorer software.

Tx PCS Lane Mapping and Skew Insertion Dialog Box

The Tx PCS physical lanes, their lane identification marker, and skew injection are specified in this port transmit dialog box. Figure 19 is the default port property's GUI configuration. The **Tx Lane** tab is shown in Figure 19.

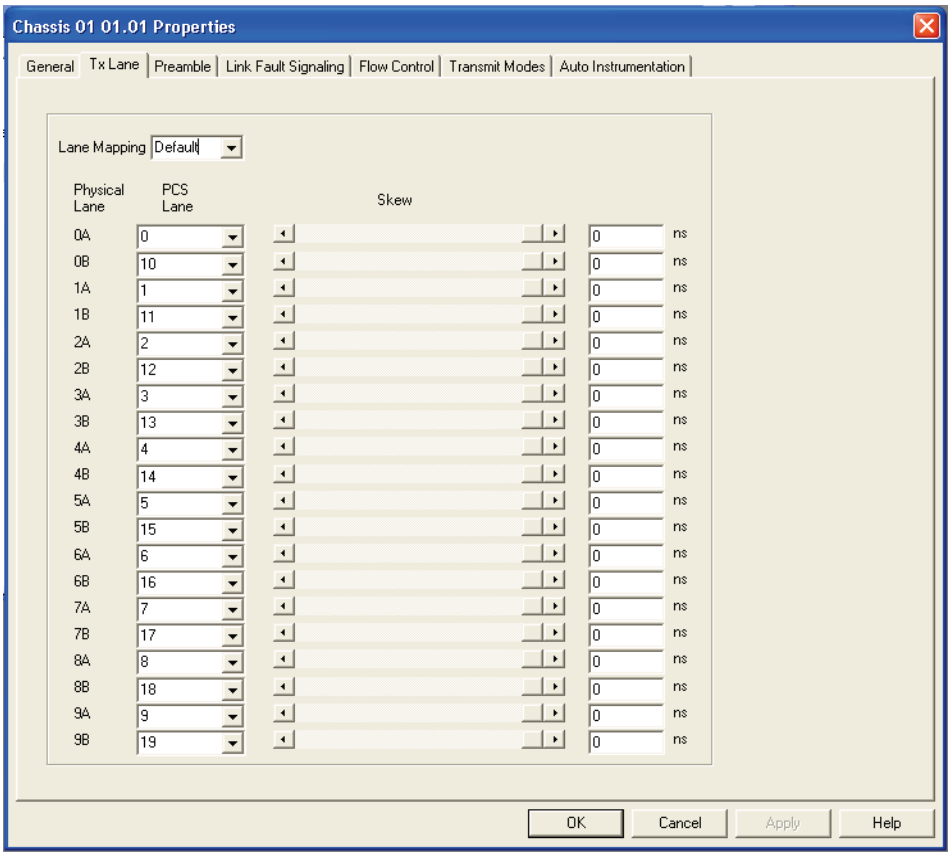


Figure 19. Ixia Tx Lane for PCS Transmit Lane mapping and skew insertion

The **PCS Lane** assignments may be edited user. Lane skew can be applied on any **Physical Lane** and in any combination. The injected Tx skew is controlled by the slider bar.

A skew of 0 is the minimum and 3 microseconds is the largest PCS Lanes skew that may be injected using the GUI slider bar controls. The Tx skew resolution is 6.206 nanoseconds. Each mouse click inserts 6.206 nanoseconds. 6.206 nanosecond is equivalent to one clock cycle of the transmit port's reference clock. The slider bar allows for the quick insertion of very large amounts of skew.

There are four methods to control the **PCS Lane** mapping:

- Default pattern – this is the initial lane map used when the port is initialized.

- Incrementing – assigns the lane mapping in ascending order.
- Decrementing – assigns the lane mapping in descending order.
- Random – Randomizes the mapping.
- Custom – any assignment of input lane map values is allowed, including duplicates.

Any of the mapping and skew controls may be applied whenever desired. The ability to test the PCS layer does not require IP traffic to be running over the link.

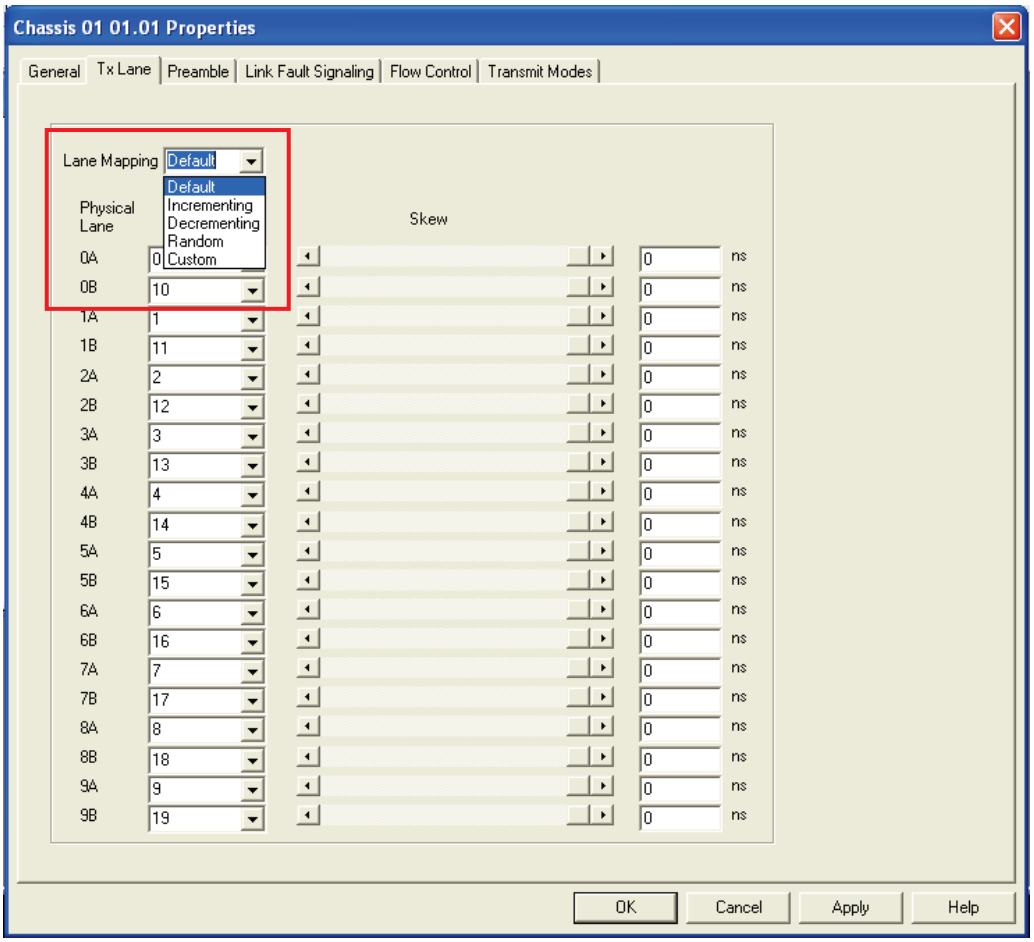


Figure 20. Ixia Tx Lanes PCS Lane mapping options

The Tx PCS lane dialog box shown in Figure 21 is a test setup with skew inserted into three different physical lanes. Deliberate lane skew can be applied to one or both PCS lanes of a physical lane and over as many PCS lanes, in any combination as desired.

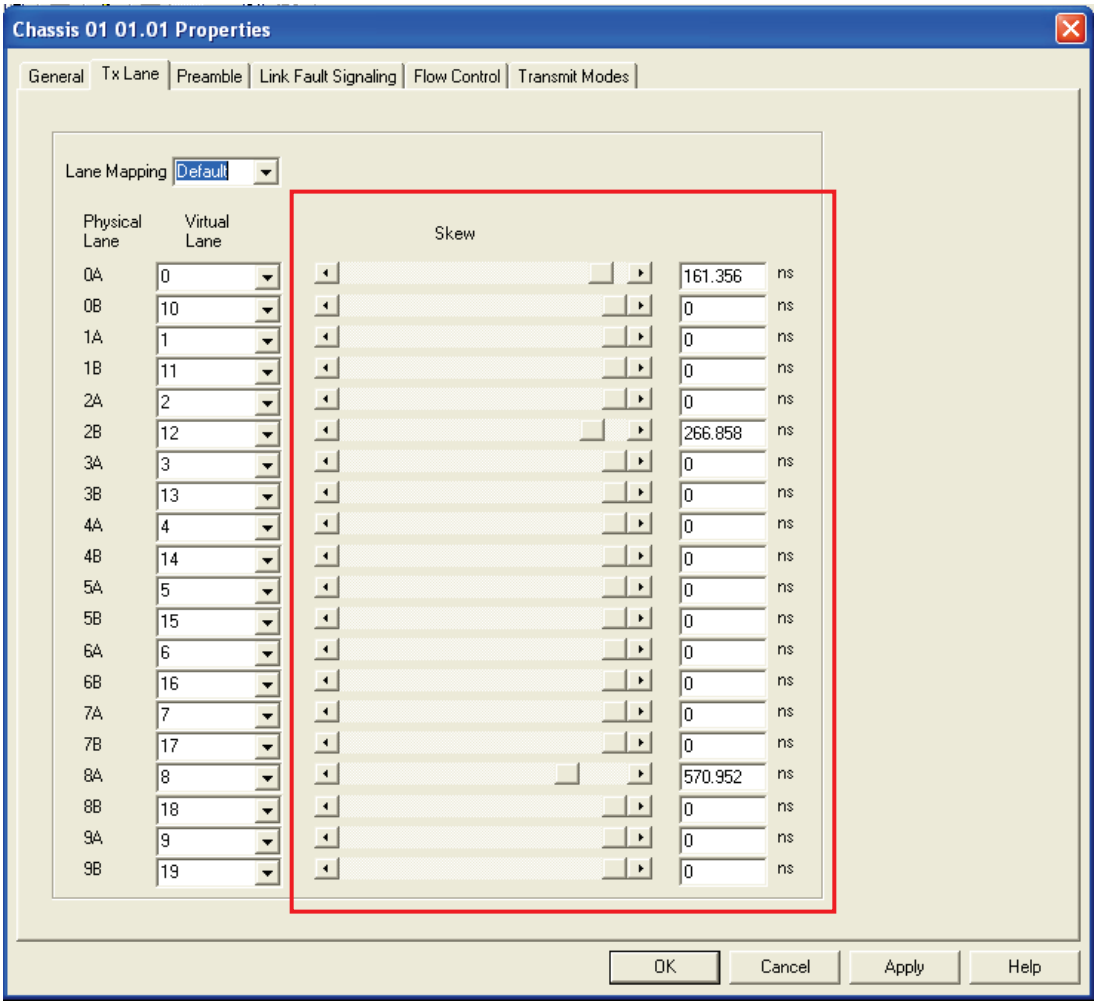


Figure 21. Ixia Tx Lane for PCS Lane skew insertion

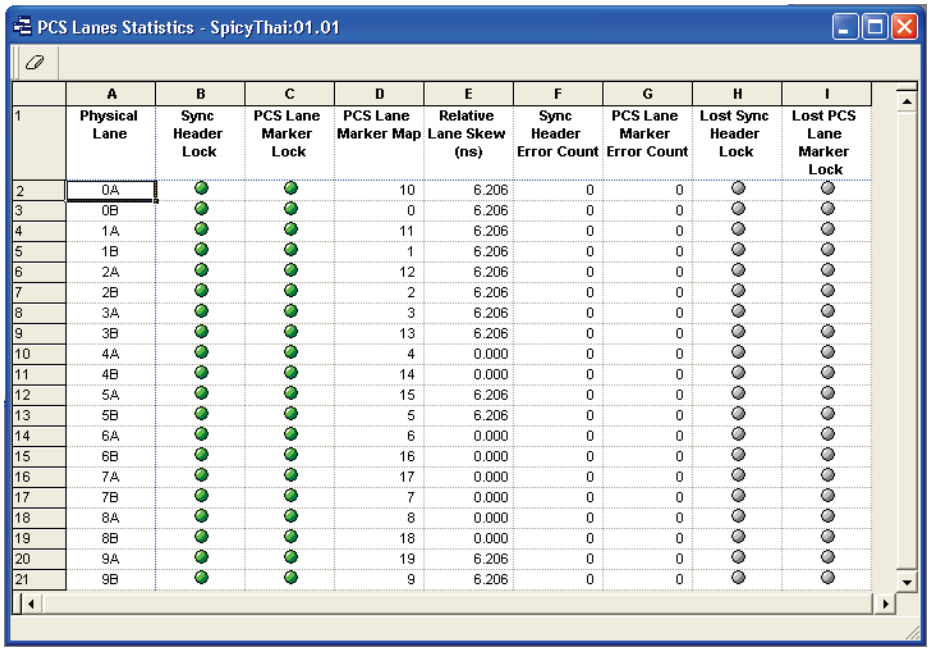
The Tx PCS lane and skew insertion configuration will remain exactly as set until it is changed, reset, or the load module is hot-swapped and/or powered off. The Tx-side configuration can be changed while a test is running and the Rx-side will immediately react and instantly refresh measurements.

Any Tx PCS lane configuration may be saved into individual test file configurations. These configurations may be recalled, applied, and executed. This is ideal for setting up test suites for repetitive and regression testing as PCS layer development occurs.

The amount of lane skew inserted in the figure above shows values that are both within and beyond the IEEE802.3ba tolerance for lane skew, which is 180 ns. The Ixia PCS layer test tool allows stress testing of the Tx and Rx-sides.

Rx PCS Lanes Statistics Dialog Box

RX side PCS lanes and statistics are automatically measured and displayed with the **PCS Lanes Statistics** dialog box. The PCS lane Rx side skew, synchronization and mapping measurements are available without IP traffic running over the link. Measurements are made at the PCS layer in real time. Link status is monitored and evaluated at all times.



	A	B	C	D	E	F	G	H	I
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			10	6.206	0	0		
3	0B			0	6.206	0	0		
4	1A			11	6.206	0	0		
5	1B			1	6.206	0	0		
6	2A			12	6.206	0	0		
7	2B			2	6.206	0	0		
8	3A			3	6.206	0	0		
9	3B			13	6.206	0	0		
10	4A			4	0.000	0	0		
11	4B			14	0.000	0	0		
12	5A			15	6.206	0	0		
13	5B			5	6.206	0	0		
14	6A			6	0.000	0	0		
15	6B			16	0.000	0	0		
16	7A			17	0.000	0	0		
17	7B			7	0.000	0	0		
18	8A			8	0.000	0	0		
19	8B			18	0.000	0	0		
20	9A			19	6.206	0	0		
21	9B			9	6.206	0	0		

Figure 22. Ixia Rx-side PCS Lanes Statistics dialog box

The PCS lanes statistics measured in this dialog box are:

- Physical and PCS lane address assignments
- Sync header lock
- PCS lane marker lock
- PCS lane marker map
- Relative lane skew
- Synch header error count
- PCS lane marker error count
- BIP-8 Error Count
- Lost synch header lock
- Lost PCS lane marker lock

Table 3. Functional description of PCS receive-side measurements and capabilities

Rx Screen Column Name	Measurement Description
Physical Lane	The identifier for the Receive physical lane. This is a tag/fixed label to identify each of the twp PCS lanes assigned to that particular Physical Lane.
Sync Header Lock	This is the 64/66B encoded block synchronization lock status that Indicates if the received PCS lane achieved sync-bit lock on the 64/66b encoded block. A Green LED indicates equals success, and a red LED indicator is a failure, or error.
PCS Lane Marker Lock	Indicates if the received PCS lane has achieved alignment marker lock. A Green LED indicates equals success, and a red LED indicator is a failure, or error.
PCS Lane Marker Map	This is the Physical Lane identification address assignment. The PCS lane number identified by the alignment marker. This is only valid when PCS Lane Marker Lock LED indicator is green.
Relative Lane Skew (ns)	Shows the actual skew in nanoseconds. Skew measurements are valid only when all lanes are locked with 20 unique lane markers, required for a 100 GE port. The first PCS Lane markers to arrive have a skew of 0. All other lane skew values are relative to the Physical Lane that locked first, before the other lanes. This may change from test to test and is part of the design dictated by the IEEE802.3ba standard. The Ixia Rx Relative Lane skew measurement system has the ability to measure skew from 0 ns up to 6 microseconds.
Synch Error Header Count	This column counts the number of errors when 64/66b encoded blocks that have lost synchronization.
PCS Lane Marker Error Count	This column counts the number of PCS lanes that are not remaining aligned to their physical lane assignment. When these PCS lanes miss their assigned Physical lane an error count is generated.
Lost Synch Header Lock	This is an LED-like indicator, grey means there are no errors, and it turns red if there are errors. This turns red when 64/66b encoded block have lost lock.
Lost PCS Lane Marker Lock	This is an LED-like indicator, grey means there are no errors, and it turns red if there are errors. This turns red when PCS Lane Markers are no longer matching their assigned Physical Lane.

Accessing the Tx and Rx PCS Lanes Dialog Screens

Accessing the Transmit PCS Lanes dialog box

The **Tx Lane** tab provides the ability to control the PCS lanes transmit configuration, including the amount of lane skew. It is part of the Ixia's load modules' **Port Properties** for both 40 and 100 Gb/s ports.

Note. The other tabs on the port properties page are described in the IxExplorer user guide, as are the rest of the controls for the chassis and load modules.

To open the **Tx Lane** dialog box:

1. Select the load module in the left pane of the IxExplorer window.
2. Select the port of the load module where the test will be executed.
3. Select Port Properties in the right hand pane of the IxExplorer window.
4. Select the Tx Lane tab. This opens the Tx PCS lane mapping and skew insertion dialog box.

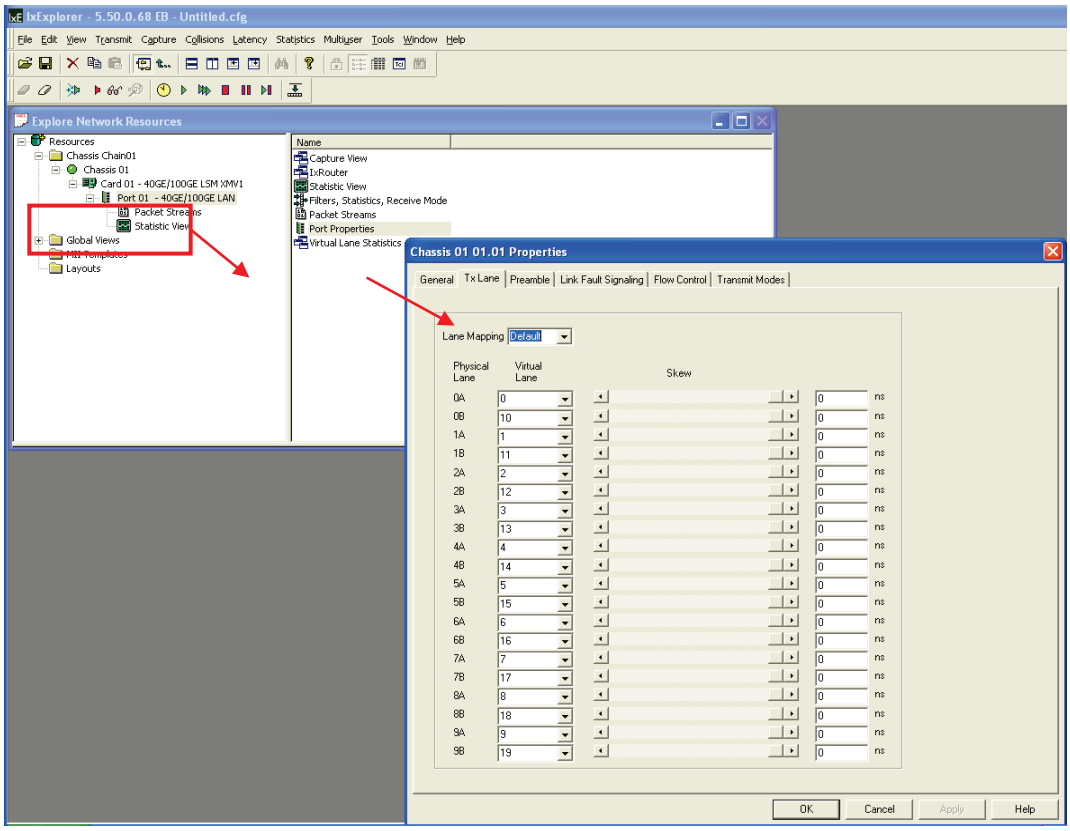


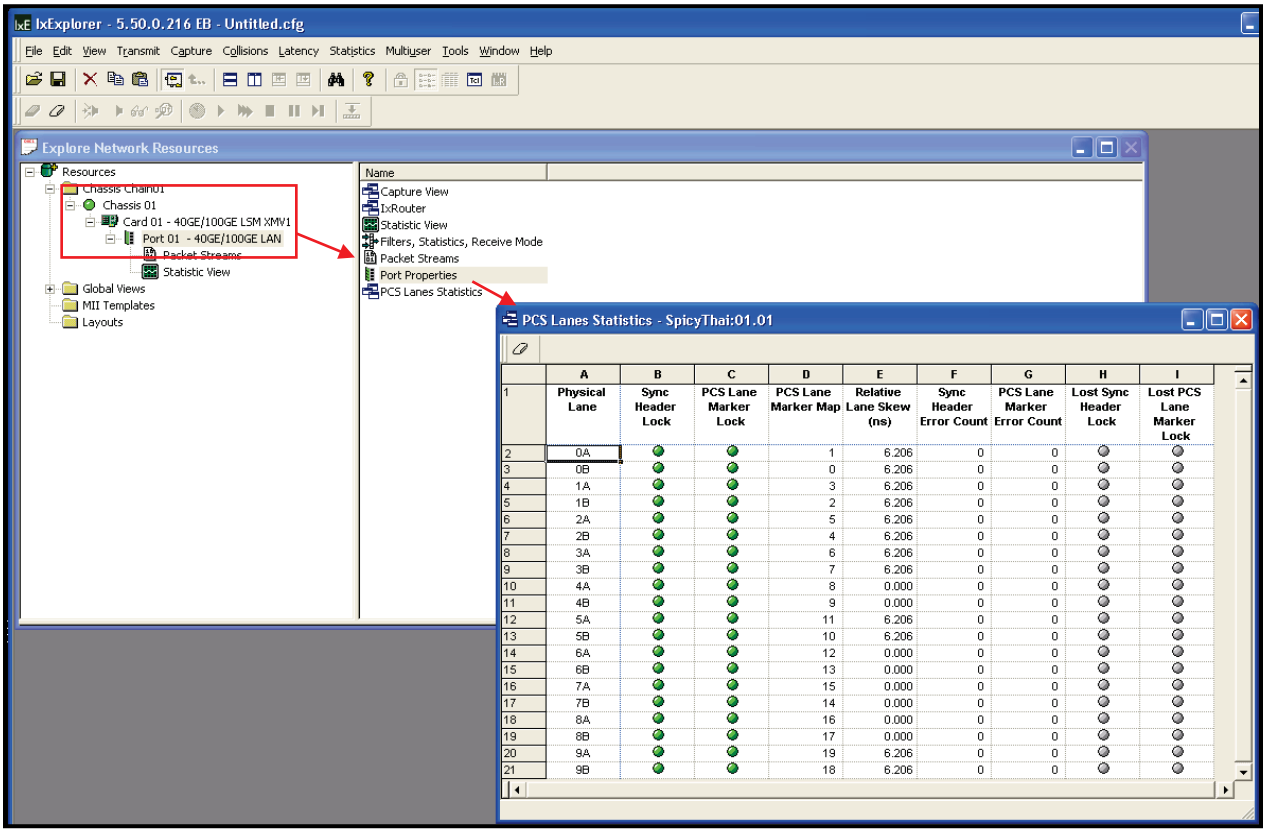
Figure 23. Accessing the Tx Lane dialog box

Accessing the Receive PCS Lanes Statistics dialog box

The **PCS Lanes Statistics** dialog box provides the ability to view Rx-side statistics, measurements, synchronizations and status indicators. It is part of the Ixia's load modules' **Port Properties** for both 40 and 100 Gb/s ports.

To open the **PCS Lanes Statistics** dialog box:

1. Select the load module in the left pane of the IxExplorer window.
2. Select the port of the load module where the test will be executed.
3. In the right pane double click the PCS Lanes Statistics. This opens the PCS Lanes Statistics dialog box.



	A Physical Lane	B Sync Header Lock	C PCS Lane Marker Lock	D PCS Lane Marker Map	E Relative Lane Skew (ns)	F Sync Header Error Count	G PCS Lane Marker Error Count	H Lost Sync Header Lock	I Lost PCS Lane Marker Lock
2	0A			1	6.206	0	0		
3	0B			0	6.206	0	0		
4	1A			3	6.206	0	0		
5	1B			2	6.206	0	0		
6	2A			5	6.206	0	0		
7	2B			4	6.206	0	0		
8	3A			6	6.206	0	0		
9	3B			7	6.206	0	0		
10	4A			8	0.000	0	0		
11	4B			9	0.000	0	0		
12	5A			11	6.206	0	0		
13	5B			10	6.206	0	0		
14	6A			12	0.000	0	0		
15	6B			13	0.000	0	0		
16	7A			15	0.000	0	0		
17	7B			14	0.000	0	0		
18	8A			16	0.000	0	0		
19	8B			17	0.000	0	0		
20	9A			19	6.206	0	0		
21	9B			18	6.206	0	0		

Figure 24. Accessing the PCS Lanes Statistics Rx-Side dialog box

This displays the condition of the Tx and Rx-sides of a single 100 GE port. In this example, an Ixia XM2 chassis has a 100 Gb/s load module installed in port loopback mode, as described earlier. The default Tx set up has been applied in the **Tx Lane** dialog box. In the Rx **PCS Lanes Statistics** dialog box all of the measurements are shown.

Examples of the PCS Layer Test System in Normal Operation

A brief review of the Tx and Rx-side PCS screens, Figure 25 and Figure 26, explain how the test system reports values when the link is perfect on a 100 Gb/s port loopback link with **Default** PCS lane mapping and no lane skew.

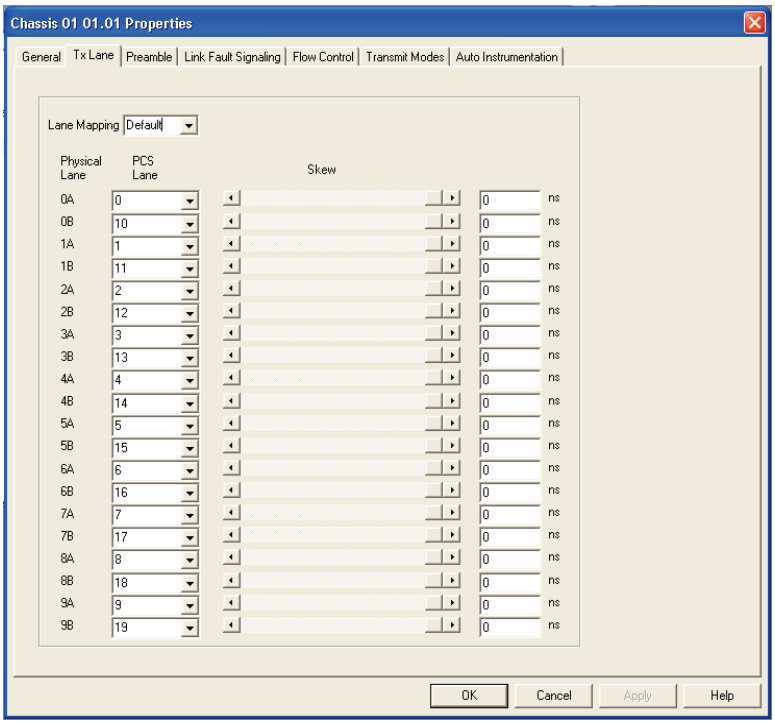
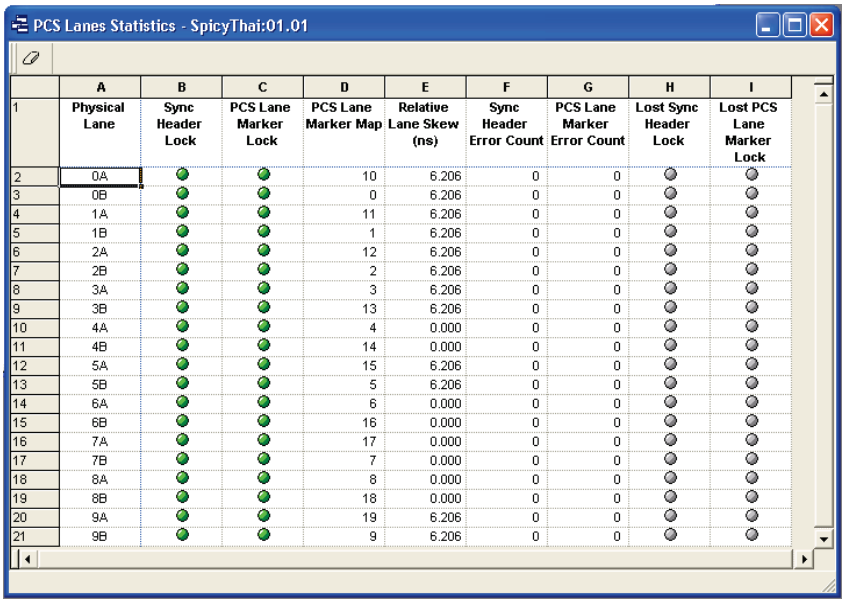


Figure 25. Tx Lane PCS Lanes dialog box with a good link



	A	B	C	D	E	F	G	H	I
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			10	6.206	0	0		
3	0B			0	6.206	0	0		
4	1A			11	6.206	0	0		
5	1B			1	6.206	0	0		
6	2A			12	6.206	0	0		
7	2B			2	6.206	0	0		
8	3A			3	6.206	0	0		
9	3B			13	6.206	0	0		
10	4A			4	0.000	0	0		
11	4B			14	0.000	0	0		
12	5A			15	6.206	0	0		
13	5B			5	6.206	0	0		
14	6A			6	0.000	0	0		
15	6B			16	0.000	0	0		
16	7A			17	0.000	0	0		
17	7B			7	0.000	0	0		
18	8A			8	0.000	0	0		
19	8B			18	0.000	0	0		
20	9A			19	6.206	0	0		
21	9B			9	6.206	0	0		

Figure 26. Rx PCS Lanes Statistics Lanes dialog box with a good link

The Rx **PCS Lanes Statistics** dialog screen shows a healthy 100 Gb/s link with no errors.

A review of the state of the each column of the **PCS Lanes Statistics** dialog box provides clarity on the PCS layer measurements and indicators when a 100 GE port has a healthy link. These screens were generated by simply plugging in the MPO fiber cable into the Tx and Rx-side s of the Ixia 100 Gb/s test port and ensuring there is a healthy link example.

PCS Lanes Statistics Measurement Example Table

Table 4. Functional description of PCS receive-side with a good link

Rx Screen Column	Measurement Description	Pass/ Fail Status and comment
Physical Lane	The identifier for the receive physical lanes. This is a tag/fixed label that IDs each physical lane. It can be seen that the Rx-side has verified that the physical lanes have been received in the transmitted order in compliance with the IEEE standard.	**Pass**.
Sync Header Lock	Indicates if the received 64B/66B encoded blocks have achieved sync-bit lock. A green LED indicates a successful synchronization, a red LED indicates a failure to synchronize.	**Pass.** The indicator is green. The link is synchronized with respect to the 64B/66B encoded blocks it received. If any PCS lane had a red LED indicator, the link will go completely down and the rating for this metric is fail until the synch is restored.
PCS Lane Marker Lock	Indicates if the received PCS lanes have achieved alignment marker lock. Green indicates a success marker lock. A red LED indicates a failure to lock onto its lane marker assignment.	**Pass.** The indicator is green. The PCS lanes have been correctly received and identified and are aligned with respect to their physical lane assignments.
PCS Lane Marker Map	The PCS lane marker numbers have been identified and aligned as expected. This is only valid when the LED indicator for the PCS lane marker lock is green.	**Pass.** A complaint lane marker mapping pattern has been received. This is an expected result on a loop-backed port. On a DUT this mapping is likely to be different as the Rx-side would measure the DUT's Tx rather than what the Ixia test tool originally transmitted to the DUT.

Rx Screen Column	Measurement Description	Pass/ Fail Status and comment
Relative Lane Skew (ns)	Shows the actual skew in nanoseconds. Skew measurements are valid only when all lanes are locked with 20 unique lane markers for a 100 Gb/s link. The first PCS lane markers to arrive have a skew of 0 ns. All other lane skew values are relative to them.	**Pass.** Physical lanes 4, 6, 7 and 8 arrived at the same time with zero lane skew. The other PCS lanes arrived after lanes 4, 6, 7 and 8 and posses a small amount of relative skew (i.e. all the lanes with the 6.206 ns of skew). All the other PCS lanes show a value of one or two clock cycles with respect to any relative reference lane. This is within the measurement tolerance of the Ixia skew measurement system. There is a clear statistics button in the upper left corner of the screen that will reset the link and bring most, if not all of the PCS lanes to a zero value for skew. The clear statistics button may be used at any time.
Synch Error Header Count	The number of synchronization bit errors received from 64/66b encoded blocks.	**Pass.** Zero errors are shown. If there are encoded sync errors detected, then the system will count them. Clear statistics may be used.
PCS Lane Marker Error Count	The number of incorrect PCS lane markers received while in PCS lane lock state.	**Pass.** Zero errors are shown. If there are PCS lane markers that are incorrect or corrupted, then the PCS lane marker errors will be counted. Clear statistics may be used.
Lost Synch Header Lock	A red LED indicates a PCS lane loss of 64B/66B sync-bit lock since the last statistic was read. If the LED indicator is colored gray, there is no error. If the LED indicator is colored red, then an error count is recorded.	**Pass.** When this indicator is gray it means that the PCS 64B/66B encoded block and sync-bit lock is operational and without error. If there were an error the indicator would go red for that lane that lost its synchronization.
Lost PCS Lane Marker Lock	A red LED indicates loss of PCS lane market lock since the last was statistic read. If the LED is colored gray, there is no error. If the LED indicator is colored red, then an error count is recorded.	**Pass.** When this indicator is gray it means that the PCS lane alignment and lock is operational and without error. If there were error the indicator would go red.

Test Case: 100 GE Broken Link and Recovery

Overview

A common test is to see if an Ethernet port with a healthy link can recover link when a cable is removed. Link recovery testing is performed by simply re-inserting the cable. A normal Ethernet port should recover link and be fully operational.

Objective

The objective of this test is to show what happens to a fully operational 100 GE link, when the link is broken between two connected ports. The port in loopback mode can demonstrate the link recovery process with its PCS lanes measurement capability.

Step by Step Instructions

1. First, setup up the Ixia 100 Gb/s test system as shown in Figure 18, in the Physical Test Topology for PCS Layer test methodology section.
2. Access the **Tx Lane** dialog box and set the **PCS Lanes** mapping to **Default** mapping order. This is shown in the Figure 27below. Refer to the Accessing the Transmit PCS Lanes dialog box section.

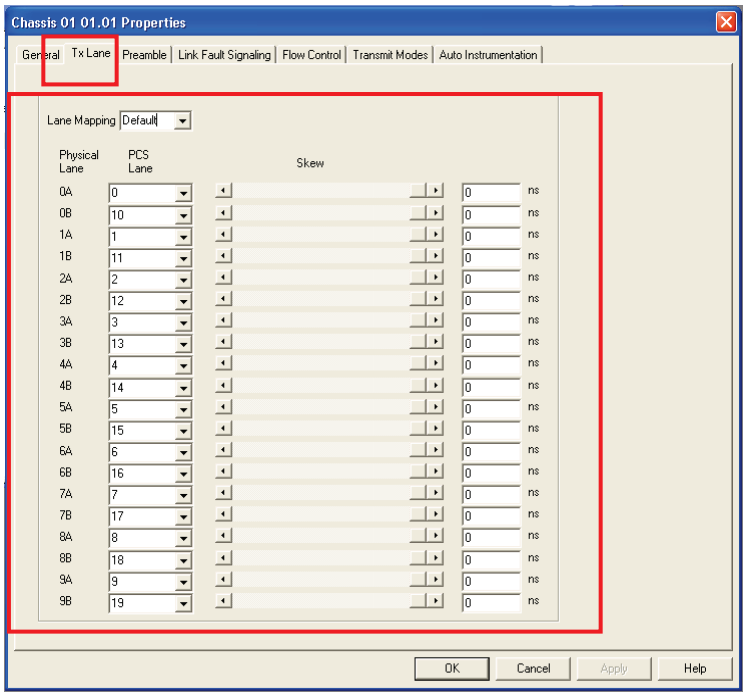


Figure 27. Tx Lane dialog box with default lane mapping order

3. Unplug the fiber ribbon cable from the Tx side port. This will cause the physical 100 Gb/s link to be broken. The 100 Gb/s link is now down.

4. Access the **PCS Lanes Statistics** dialog box to view the Rx-side results. Refer to the Accessing the Receive PCS Lanes Statistics dialog box section.

5. Stop and review the state and measurements of the **Receive PCS Lanes Statistics** dialog box in the **Results Analysis** section.

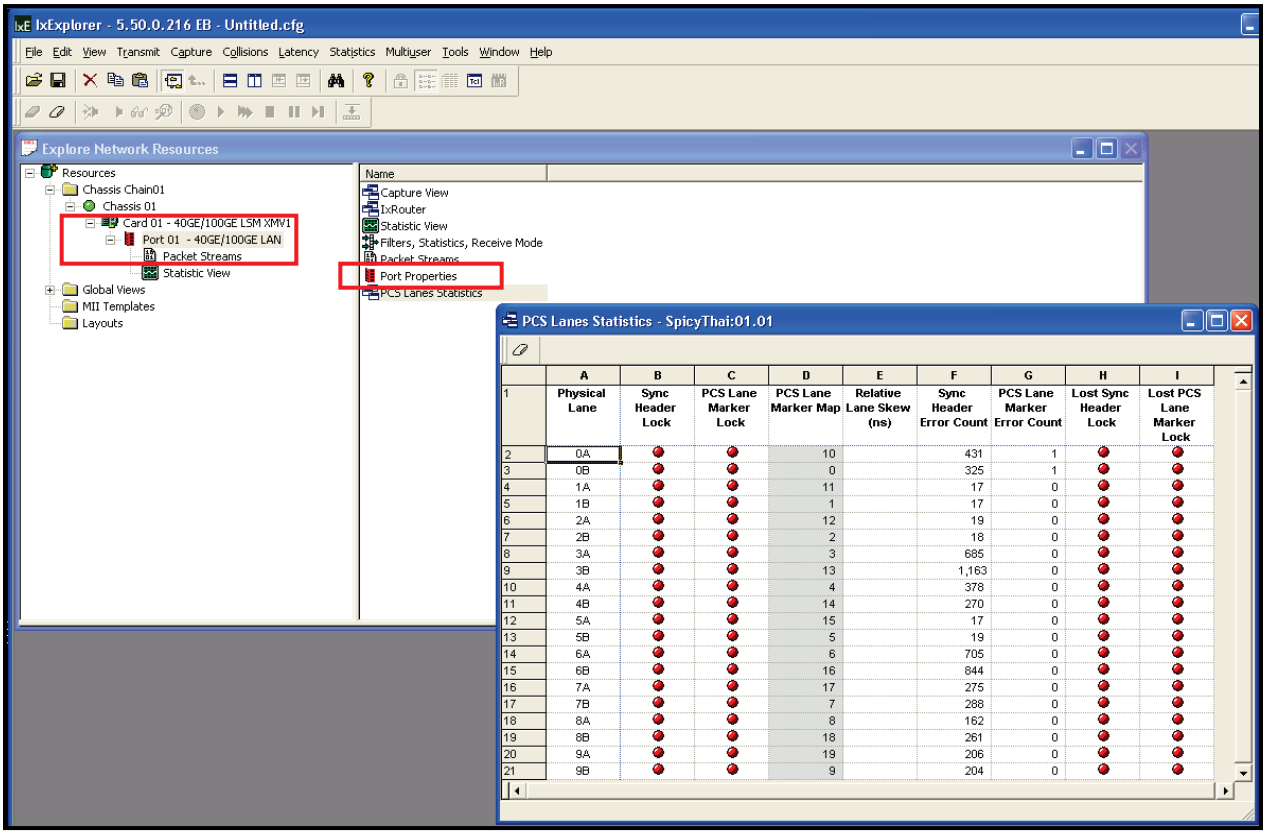
6. Plug the fiber ribbon cable back into the transmit port. This completes the test and the final result of the link recovery is shown in the **Results Analysis** section that follows.

Results Analysis

The **PCS Lanes Statistics** dialog box shows what happens when the fiber cable is simply removed from the transmit side port while the Ixia 100 Gb/s test system was sending line rate 100 Gb/s layer-2 traffic with 64-byte frame lengths. See Figure 28.

Note: IP traffic was running over the link before the link was broken. However, to run this test IP traffic is not required to simulate the link conditions shown below.

The red boxes show the indicators in IxExplorer's left and right panes alert the user that the link is down. The **PCS Lanes Statistics** LED indicators are all red, which indicates that the link is down.



	A Physical Lane	B Sync Header Lock	C PCS Lane Marker Lock	D PCS Lane Marker Map	E Relative Lane Skew (ns)	F Sync Header Error Count	G PCS Lane Marker Error Count	H Lost Sync Header Lock	I Lost PCS Lane Marker Lock
2	0A			10		431	1		
3	0B			0		325	1		
4	1A			11		17	0		
5	1B			1		17	0		
6	2A			12		19	0		
7	2B			2		18	0		
8	3A			3		685	0		
9	3B			13		1,163	0		
10	4A			4		378	0		
11	4B			14		270	0		
12	5A			15		17	0		
13	5B			5		19	0		
14	6A			6		705	0		
15	6B			16		844	0		
16	7A			17		275	0		
17	7B			7		288	0		
18	8A			8		162	0		
19	8B			18		261	0		
20	9A			19		206	0		
21	9B			9		204	0		

Figure 28. PCS Lanes Statistics dialog box with a broken link

A key point is that despite losing link the Ixia PCS lanes statistics test system does not go down. It will recover link even in an extreme error, such as the removal of the cable or a broken fiber on the link.

A review of the **PCS Lanes Statistics** Table 5 will explain what the screen with the broken link shows. The explanation clarifies the behavior of the 100 Gb/s test system.

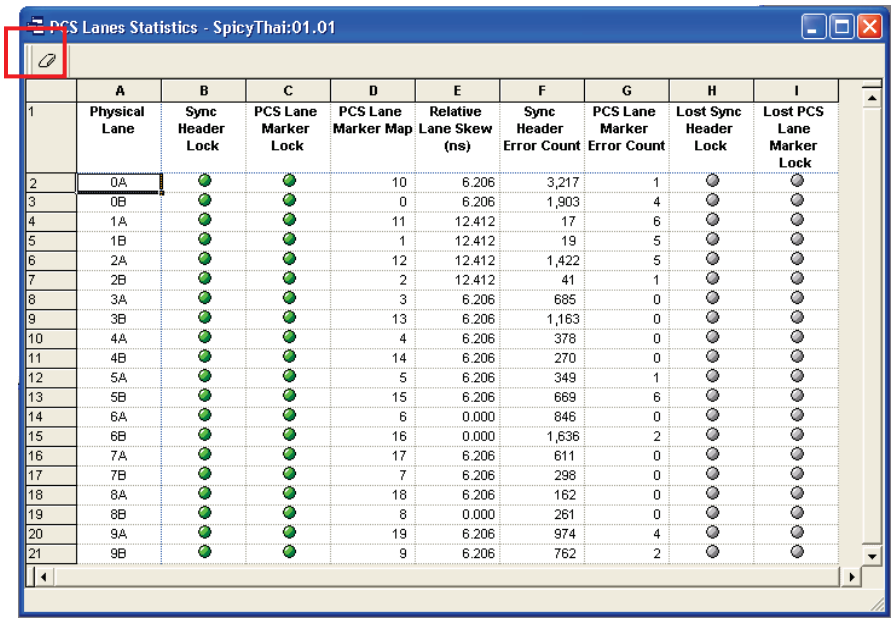
Table 5. Broken link: PCS Lanes statistics measurement example table

Rx Screen Column	Measurement Description	Pass/ Fail Status and comment
Physical Lane	The receive side identifier physical lanes. This is a tag/fixed label that IDs each physical lane. The Rx-side has verified that the physical lanes have been received in the transmitted order in compliance.	**Pass**.
Sync Header Lock	Indicates if the received 64B/66B encoded blocks have achieved sync-bit lock. A green LED indicates a successful synchronization, a red LED indicates a failure to synchronize.	**Fail.** All the indicators are red. The link is not synchronized with respect to the 64B/66B encoded blocks it received.
PCS Lane Marker Lock	Indicates if the received PCS lanes have achieved alignment marker lock. Green indicates a success marker lock. A red LED indicates a failure to lock onto its lane marker assignment.	**Fail.** All the indicators are red. The PCS lanes have not been correctly received and identified with respect to their physical lane assignment.
PCS Lane Marker Map	The PCS lane marker numbers have been identified and aligned as expected. This is only valid when the LED indicator for the PCS lane marker lock is green.	**Pass.** They were transmitted in a compliant default mapping order.
Relative Lane Skew (ns)	Shows the actual skew in nanoseconds. Skew measurements are valid only when all lanes are locked with 20 unique lane markers. The first PCS lane markers to arrive have a skew of 0 ns. All other lane skew values are relative to them.	**Fail.** No PCS lanes met the marker ID verification test and are no longer arriving; therefore no skew was measured and reported.
Synch Error Header Count	The number of synchronization bit errors received from 64/66b encoded blocks.	**Fail.** When the entire link is broken every lane has PCS bit sync errors detected and the test system counted and reported them. The clear statistics button can be used to reset the statistics.
PCS Lane Marker Error Count	The number of incorrect PCS lane markers received while in PCS lane lock state.	**Pass.** Most PCS lane markers are zero, indicating that the link was broken while the counting system was renewing itself. PCS lane marker errors are counted. The clear statistics button can be used to reset the statistics.

Rx Screen Column	Measurement Description	Pass/ Fail Status and comment
Lost Synch Header Lock	A red LED indicates a PCS lane loss of 64B/66B sync-bit lock since the last statistic was read. If the LED indicator is colored gray, there is no error. If the LED indicator is colored red, then an error count is recorded.	**Fail.** All the LED indicators are red. It means that the PCS 64B/66B sync-bit lock is not operational and has many errors.
Lost PCS Lane Marker Lock	A red LED indicates loss of PCS lane market lock since the last was statistic read. If the LED is colored gray, there is no error. If the LED indicator is colored red, then an error count is recorded.	**Fail.** All the indicators are red. It means that the PCS lane marker alignment and lock is not operational and has errors.

RX-side PCS lanes statistics measurement recovers from broken link

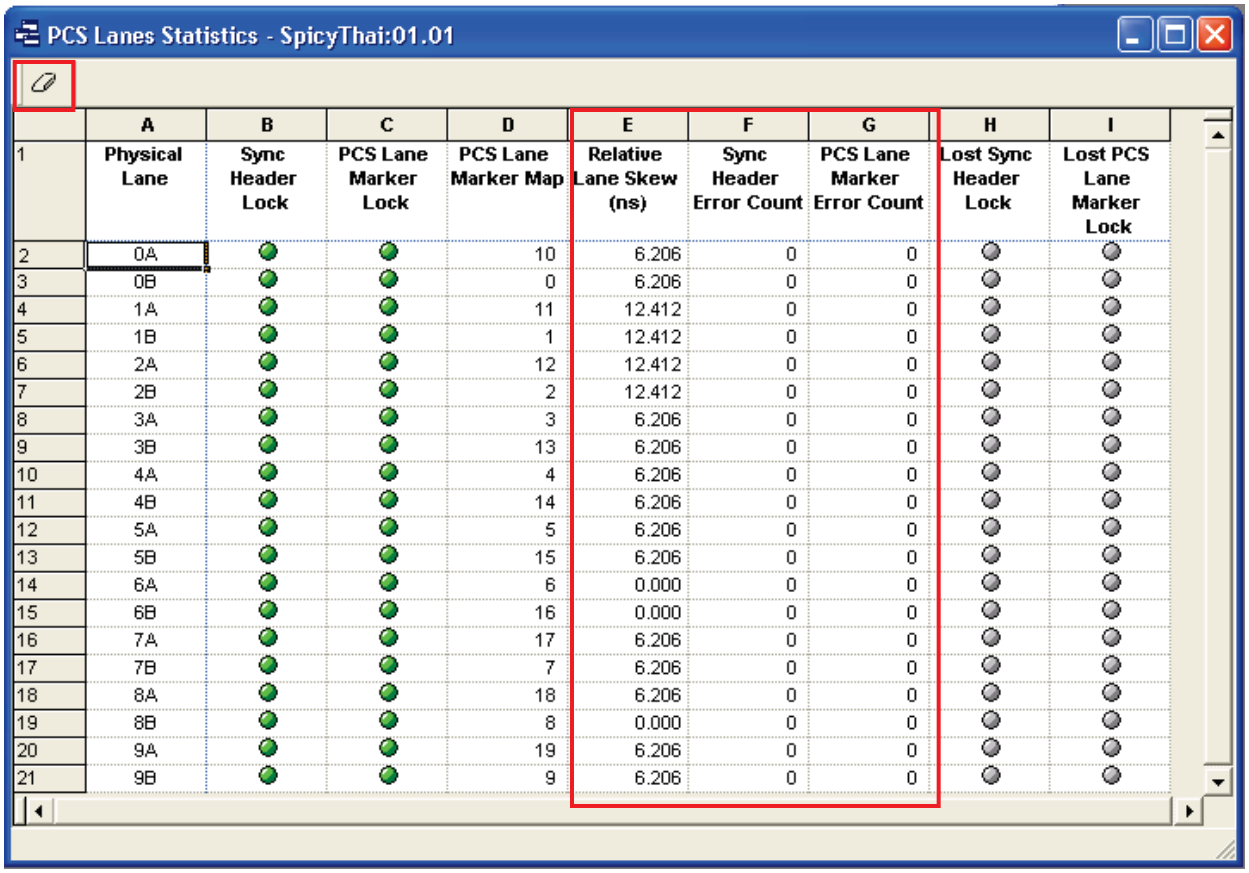
In step 6, the fiber ribbon cable has been plugged back into the transmit port. The Ixia test system re-starts the process of establishing 64B/66B synchronization bit lock, and PCS lane marker alignment and marker lock. The test system recovers and brings the link back up with all lock LED indicators green. The **Sync Header Lock** and **PCS Lane Marker Lock** LED indicators are gray. The key point is that the error counts columns retain the reported errors counted up to when the link is restored. Statistics must be cleared by the **Clear Statistics Icon** button in the upper left corner of the dialog box.



	A	B	C	D	E	F	G	H	I
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			10	6.206	3,217	1		
3	0B			0	6.206	1,903	4		
4	1A			11	12.412	17	6		
5	1B			1	12.412	19	5		
6	2A			12	12.412	1,422	5		
7	2B			2	12.412	41	1		
8	3A			3	6.206	685	0		
9	3B			13	6.206	1,163	0		
10	4A			4	6.206	378	0		
11	4B			14	6.206	270	0		
12	5A			5	6.206	349	1		
13	5B			15	6.206	669	6		
14	6A			6	0.000	846	0		
15	6B			16	0.000	1,636	2		
16	7A			17	6.206	611	0		
17	7B			7	6.206	298	0		
18	8A			18	6.206	162	0		
19	8B			8	0.000	261	0		
20	9A			19	6.206	974	4		
21	9B			9	6.206	762	2		

Figure 29. PCS Lanes Statistics with a recovered link

After the PCS Lanes Statistics dialog box has been cleared, it will display itself as shown in the preceding figure. Review the red box highlights. **Sync Header Errors** and **PCS Lane Marker Error** counts are restored to a zero count. A key point is that we see the return of **Relative Lane Skew** values with the re-establishment of the link. All are within the one or two clock count tolerance for the lane skew measurement system.



	A	B	C	D	E	F	G	H	I
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			10	6.206	0	0		
3	0B			0	6.206	0	0		
4	1A			11	12.412	0	0		
5	1B			1	12.412	0	0		
6	2A			12	12.412	0	0		
7	2B			2	12.412	0	0		
8	3A			3	6.206	0	0		
9	3B			13	6.206	0	0		
10	4A			4	6.206	0	0		
11	4B			14	6.206	0	0		
12	5A			5	6.206	0	0		
13	5B			15	6.206	0	0		
14	6A			6	0.000	0	0		
15	6B			16	0.000	0	0		
16	7A			17	6.206	0	0		
17	7B			7	6.206	0	0		
18	8A			18	6.206	0	0		
19	8B			8	0.000	0	0		
20	9A			19	6.206	0	0		
21	9B			9	6.206	0	0		

Figure 30. PCS Lanes Statistics with a recovered link, cleared errors, and skew values

Conclusions

The Ixia 100 Gb/s PCS measurement system can be used to measure values with or without a link. The PCS and link test system has the ability to stress test the robustness of link on the DUT and to recover from extreme PCS and link test cases that exceed the tolerance of the IEEE 802.3ba standard.

Test Case: PCS Transmit Lane Mapping and Rx-Side Measurement

Overview

The examples in test methodology two demonstrate random mapping of PCS transmit patterns within a set of three different layer 2 switches. It is a simulation of what will occur when 40 and 100 Gb/s switches are inter-connected in a real data center. Please reference Figure 31.

Two different switches, named **A** and **B**, will transmit two different PCS lane mapping patterns to a single switch named **C**. Switch C receives both patterns and must simultaneously handle both patterns on two of its 100 Gb/s ports. All of this must be accomplished within the constraints and tolerances imposed by the IEEE 802.3ba standard.

Objective

This test methodology uses the Ixia 100 GE test system in a single port loopback topology. The 100GE test system is configured two times to create multiple transmit PCS lanes setups and multiple receive PCS lanes statistics setups. The objective is to demonstrate the receive-side principles of the PCS mechanism in this test case example. The test uses multiple screen shots and data tables to accomplish the presentation and analysis of an inter-switch topology.

Step by Step Instructions

Both of the PCS lane mapping patterns from switch A and B are transmitted to switch C's Rx 100GE ports. The Ixia 100 Gb/s test system demonstrates its compliance to the HSE standard by performing real receive measurements as switch C, in the simulation.

1. First, setup up the Ixia 100 Gb/s test system as shown in Figure 18, in the Physical Test Topology for PCS Layer test methodology section. The 100 Gb/s loopback test system is used to create two random transmit patterns simulating switch and A and B, and to generate the two corresponding receive PCS lanes statistics for switch C.

2. Access the **Tx Lane** dialog box and set the **PCS lanes** mapping to **Random** PCS Lane mapping order. This is shown in Figure 32 and Figure 33 below, first for switch **A** and then for switch **B**. Refer to the **Accessing the Transmit PCS Lanes** dialog box section for an explanation of this dialog's fields.

3. There will be no lane skew in this test for switches **A** and **B**.

4. Apply the **Tx Lane Random** PCS lane mapping configuration from switch **A** to switch **C** (i.e. this is really the Rx-side of the Ixia 100 Gb/s test tool). Capture the Rx-side PCS lanes statistics dialog box, as shown in Figure 34 below.

5. Apply the **Tx Lane Random** PCS lane mapping configuration from switch **B** to switch **C** (i.e. this is really the Rx-side of the Ixia 100 Gb/s test tool). Capture the Rx-side PCS lanes statistics dialog box, as shown in Figure 35 below.

6. The next part of the test case will use the Rx-side statistics measurement to show how switch C handled these different transmit patterns on its receive side.

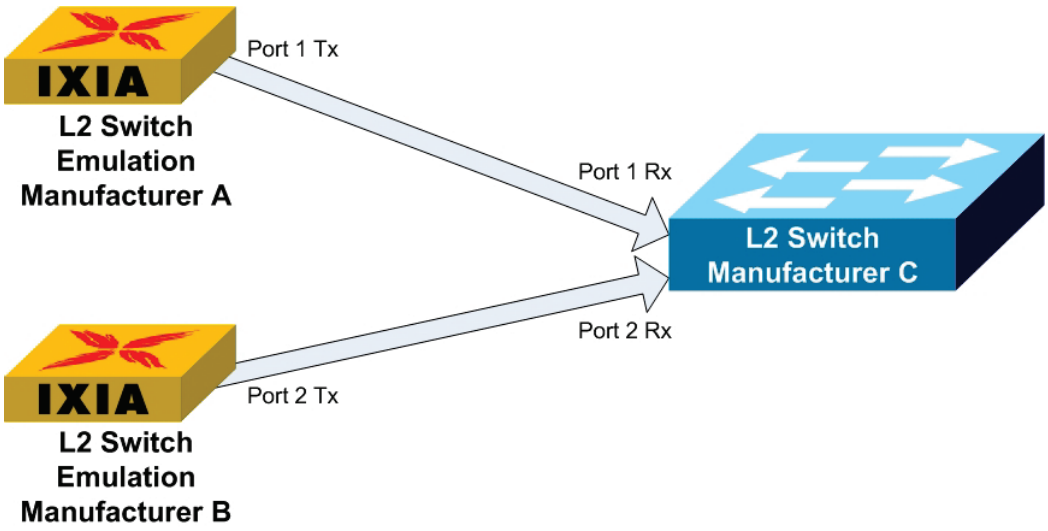


Figure 31. Test topology diagram for test methodology 2

Results Analysis

First, review the transmit patterns for switch A and switch B. Both of these patterns were set up with the test ports by using the **Random** PCS Lane mapping selection. See Figure 32 and Figure 33.

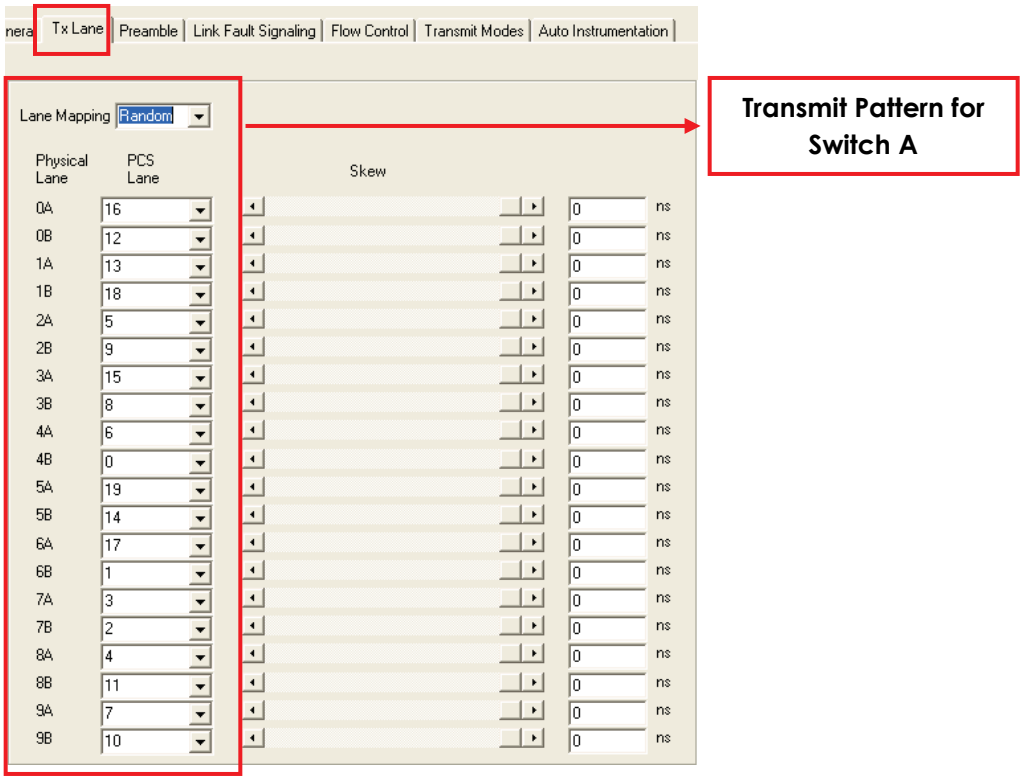


Figure 32. Tx Lane transmit random lane mapping pattern for switch A

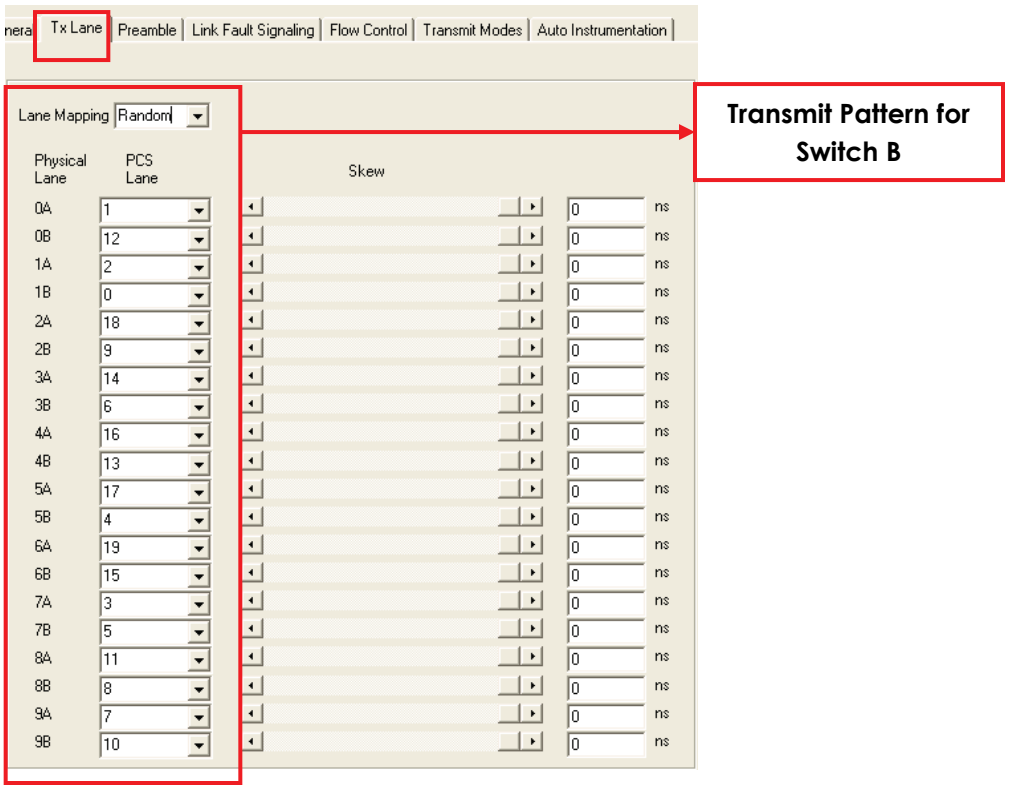


Figure 33. Tx Lane transmit random lane mapping pattern for switch B

Scanning down the 0A to 9B **Physical Lanes** of switch **A** and switch **B**, we see that both transmit PCS lanes have different mapping patterns with respect to their assignment to their physical Lanes. These were deliberate set ups for both switch A and B to emulate real world network conditions.

Switch B must be able to receive different patterns from switches **A** and **B,** and synchronize and recombine them to maintain link. Switch **C** must accomplish this in a complaint manner to the IEEE standard. See Figure 34 and Figure 35.

A	B	C	D	E	F	G	H	I
Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
0A	●	●	16	6.206	0	4	○	○
0B	●	●	12	6.206	0	4	○	○
1A	●	●	18	0.000	0	4	○	○
1B	●	●	13	0.000	0	4	○	○
2A	●	●	5	0.000	0	4	○	○
2B	●	●	9	0.000	0	4	○	○
3A	●	●	8	0.000	0	4	○	○
3B	●	●	15	0.000	0	4	○	○
4A	●	●	6	0.000	0	4	○	○
4B	●	●	0	0.000	0	4	○	○
5A	●	●	14	0.000	0	4	○	○
5B	●	●	19	0.000	0	4	○	○
6A	●	●	17	0.000	0	4	○	○
6B	●	●	1	0.000	0	4	○	○
7A	●	●	3	0.000	0	4	○	○
7B	●	●	2	0.000	0	4	○	○
8A	●	●	4	0.000	0	4	○	○
8B	●	●	11	0.000	0	4	○	○
9A	●	●	10	6.206	0	4	○	○
9B	●	●	7	6.206	0	4	○	○

Switch C, Port 1 Rx display of Switch A's Port 1 transmit.

Figure 34. PCS Lanes statistics measured from port 1 of switch A

A	B	C	D	E	F	G	H	I
Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
0A	●	●	1	6.206	0	4	○	○
0B	●	●	12	6.206	0	0	○	○
1A	●	●	0	0.000	0	4	○	○
1B	●	●	2	0.000	0	4	○	○
2A	●	●	18	0.000	0	4	○	○
2B	●	●	9	0.000	0	0	○	○
3A	●	●	6	0.000	0	4	○	○
3B	●	●	14	0.000	0	4	○	○
4A	●	●	16	0.000	0	4	○	○
4B	●	●	13	0.000	0	4	○	○
5A	●	●	4	0.000	0	4	○	○
5B	●	●	17	0.000	0	4	○	○
6A	●	●	19	0.000	0	4	○	○
6B	●	●	15	0.000	0	4	○	○
7A	●	●	3	0.000	0	0	○	○
7B	●	●	5	0.000	0	4	○	○
8A	●	●	11	0.000	0	4	○	○
8B	●	●	8	0.000	0	4	○	○
9A	●	●	10	6.206	0	0	○	○
9B	●	●	7	6.206	0	0	○	○

Switch C, Port 2 Rx display of Switch B's Port 1 transmit.

Figure 35. PCS Lanes statistics measured from port 1 of switch B

The following table compares the results from all three switches in the test. The transmit patterns from switches **A** and **B** are compared side-by-side to the Rx-side port reception of switch **C**. Some subtle but important differences between the Tx-side and the Rx-sides are highlighted in light green. Bright green is used to highlight the received PCS lane mapping values as switch **C** re-maps and recombines them.

Table 6. Comparison of test data from switches A, B, and C

Physical lanes	Switch A Transmit Port 1	Switch C Receive Port 1	Switch B Transmit Port 2	Switch C Receive Port 2
0A	16	16	1	1
0B	12	12	12	12
1A	13	18	2	0
1B	18	13	0	2
2A	5	5	18	18
2B	9	9	9	9
3A	15	8	14	6
3B	8	15	6	14
4A	6	6	16	16
4B	0	0	13	13
5A	19	14	17	4
5B	14	19	4	17
6A	17	17	19	19
6B	1	1	15	15
7A	3	3	3	3
7B	2	2	5	5
8A	4	4	11	11
8B	11	11	8	8
9A	7	10	7	10
9B	10	7	10	7

Why are the PCS lane mapping values in the green highlighted areas different on switch **C**'s Rx-side than the patterns sent from switches **A** and **B**? The PCS lane mapping assignment to the physical lanes is reversed in all of the green highlighted areas in the summary table.

A close look at the following table shows that on physical lane **1A** and **1B** PCS Lanes **13** and **18** were mapped in that order on the transmit-side. Switch C received switch **A**'s lane mapping pattern and ended up reversing it. Switch B placed PCS lane **18** where **13** was and placed lane **13** where lane **18** was originally assigned.

Table 7. Example of reversed lane mapping switch A and C

Physical lanes	Switch A Transmit Port 1	Switch C Receive Port 1
1A	13	18
1B	18	13

This is due to the bit-interleaving mechanism used to assign PCS lanes to a physical lane 1. The IEEE standard allows this reversal to take place as long as lanes 13 and 18 remain mapped to physical lane 1.

For example, if lanes 13 and 18 were suddenly mapped to a different physical lane, lane 3 perhaps, a lane marker error would occur and if it continued long enough would cause a loss of lane marker lock. This would eventually disrupt the 64B/66B encoded block synchronization and cause the link to go down.

Conclusions

The most important point that test methodology 2 demonstrates is that the Ixia test systems can be used to verify that a switch or other network device is capable of receiving any standard compliant PCS lanes transmit pattern. The test system can generates as many lane mapping cases as desired and can be used to independently verify that the DUT is compliant to the IEEE standard. The Rx-side measurement capabilities monitor all of the required elements that are used by any HSE network device to establish and maintain a link.

Test Case: PCS Lane Skew Insertion and Measurement

Overview

The test system provides the ability to inject PCS lane skew onto one or more of the PCS lanes. PCS lane skew is the injection of a time delay in increments of one clock period. A clock period, as previously discussed in the Getting Started section, is equal to 6.206 nanoseconds in time.

An easy way to visualize lane skew is to consider that the test system is delaying the start time for the test port's transmission for any chosen lane. Data transmitted from the PCS lanes to the receiving DUT Rx port becomes staggered in time.

The IEEE 802.3ba standard allows a maximum tolerance of 180 ns of skew between all the PCS lanes in a transmission. The Rx-side must be able to tolerate receiving lanes with up to 180 ns of skew delay and still keep the link up and operating correctly.

Objectives

This test case demonstrates the injection of PCS lane skew into transmissions. The receiving side then measures and reports the skew. The test case is deliberately exaggerated to demonstrate the robustness of the Ixia test system when sending, receiving, and measuring lane skew for a 100 Gb/s multimode fiber link (SNAP12).

In a real world network, lane skew is inevitable. Thus, all HSE network devices should be tested prior to deployment to independently verify that the devices meet or exceed the PCS lane skew tolerance set by the IEEE 802.3ba standard.

Step by Step Instructions

This test case will use screen shots of the Tx Lane dialog and PCS Lanes Statistics dialog boxes to demonstrate lane skew.

1. First, set up the test system as shown in Figure 18, in the Physical Test Topology for PCS Layer test methodology section. This is the platform for this test methodology.

2. Access the **Tx Lane** dialog box and set the **PCS Lanes** mapping to the **Increment PCS Lane** mapping order (Figure 35) Refer to the Accessing the Transmit PCS Lanes dialog box section.

3. In the following figure, the lane skew for this test is applied to all of the lanes. Notice that some of the lane skew values are above the 180 tolerance defined by the IEEE standard, and others are below. Apply lane skews in a pattern similar to that of Figure 36.

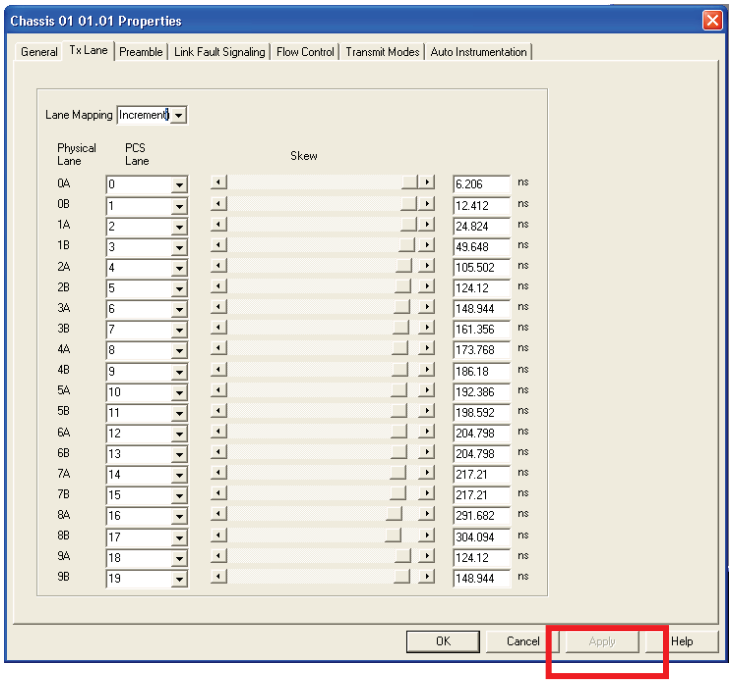
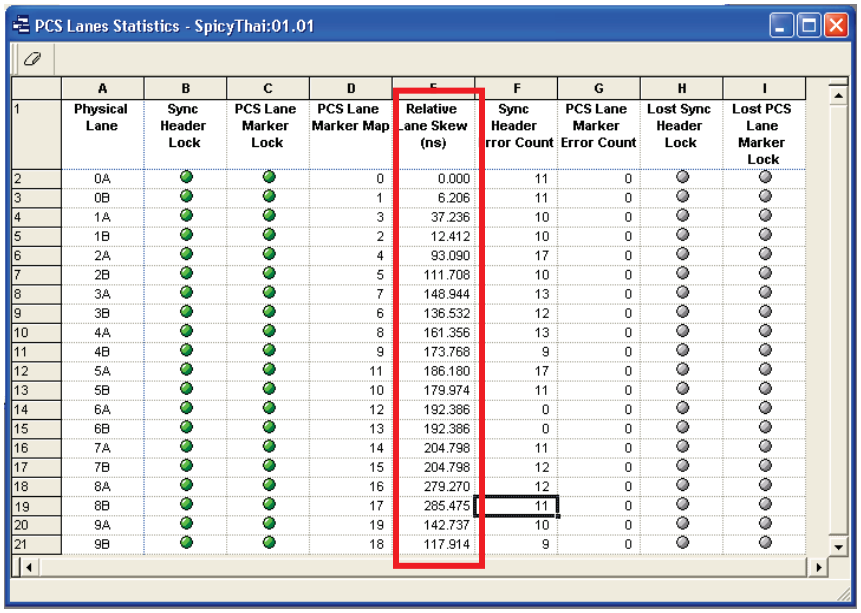


Figure 36. Applying lane skew to all transmit PCS Lanes

4. Next, capture the Rx-side of the PCS Lanes Statistics dialog box as shown in Figure 37.

5. The Rx-side PCS Lanes Statistics dialog box immediately measures the lane skew in real time. If the DUT is robust it will be able to handle these amounts of skew and not drop the HSE link. The measured lane skew shown in Figure 37 is highlighted in red under the **Relative Lane Skew (ns)** column.



	A	B	C	D	E	F	G	H	I
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			0	0.000	11	0		
3	0B			1	6.206	11	0		
4	1A			3	37.236	10	0		
5	1B			2	12.412	10	0		
6	2A			4	93.090	17	0		
7	2B			5	111.708	10	0		
8	3A			7	148.944	13	0		
9	3B			6	136.532	12	0		
10	4A			8	161.356	13	0		
11	4B			9	173.768	9	0		
12	5A			11	186.180	17	0		
13	5B			10	179.974	11	0		
14	6A			12	192.386	0	0		
15	6B			13	192.386	0	0		
16	7A			14	204.798	11	0		
17	7B			15	204.798	12	0		
18	8A			16	279.270	12	0		
19	8B			17	285.475	11	0		
20	9A			19	142.737	10	0		
21	9B			18	117.914	9	0		

Figure 37. PCS Lanes Statistics with measured lane skew and ascending lane mapping order

Results Analysis

Figure 37 shows the measured lane skew at the receiving side for each PCS lane. All of the measurements are within two clock periods (i.e. 12.412 nanoseconds) or less, compared to the amount of skew injected by the transmit port. Notice that all the LED indicators (columns **B**, **C**, **G**, and **H**) are lit green or gray, as they should be for a healthy HSE link.

There were no errors detected in the **PCS Lane Market Error Count** column. This means that each of the lanes transmitted correctly over its assigned physical lane.

The errors that are seen in the **Sync Header Error Count** show how many PCS Lane 64B 66B encoded block bit-synchronization errors occurred during the time when the lane skew was applied plus the time it took to restore the link. These errors are expected because there were different arrival times at the Rx-side across all of the lanes. This caused varying synchronization time frames per lane, to re-synchronize and restore the link. The delays that the RX-side sees reflect the number of 64B 66B errors Ixia measured as it maintained the 100 Gb/s link.

Conclusions

Test methodology 3 shows how to inject lane skew on one or more of the PCS lanes. Ixia can apply this test function to both 40 GE and 100 GE links that use 10 Gb/s x N lanes to transmit and receive. This capability can be used to test any network device for compliance to the standard and to perform stress and negative tests using a wide range of PCS lane skew configurations and skew values.

Test Case: Skew Adjustment Range and Rx-side Measurement

Overview

The Ixia HSE test system provides a maximum of 3 microseconds (i.e. 3000 nanoseconds) of PCS lane skew insertion from within the Tx Lane dialog box. On the Rx-side in the PCS Lanes Statistics dialog box, it can withstand up to 6 microseconds (i.e. 6000 nanoseconds) of lane skew and still maintain the link and continue to measure.

Objective

When a new Higher Speed Ethernet network product design is in the early stages of implementation in electronic hardware, there may be initial errors. These may show up in PCS lane testing, especially errors caused by timing and errors in the state machine that tracks the processes that manage PCS and the link.

The Ixia HSE test system is designed to interoperate with an early design network device that has errors and/or does not quite yet meet the requirements in the IEEE HSE standard. An HSE test tool must be able to interoperate even when its link partner is not working as designed or intended.

Test methodology 4 demonstrates Ixia transmit and receive lane skew tolerances that are managed by the IxExplorer test software.

Step by Step Instructions

This test case will use screen shots of the Tx Lane dialog and PCS Lanes Statistics dialog boxes to demonstrate range of lane skew available to the user.

1. First, set up the test system as shown in Figure 18, in the Physical Test Topology for PCS Layer test methodology section. This is the platform for this test methodology.
2. Access the **Tx Lane** dialog box and set the **PCS Lanes** mapping to the **Incrementing** mapping order. (Figure 38) Any of the mapping settings may be used for this test case. Refer to the Accessing the Transmit PCS Lanes dialog box section.

3. Set the **Skew** adjustment as shown in Figure 38. **Apply** the Tx PCS Lanes incremental mapping and skew values.

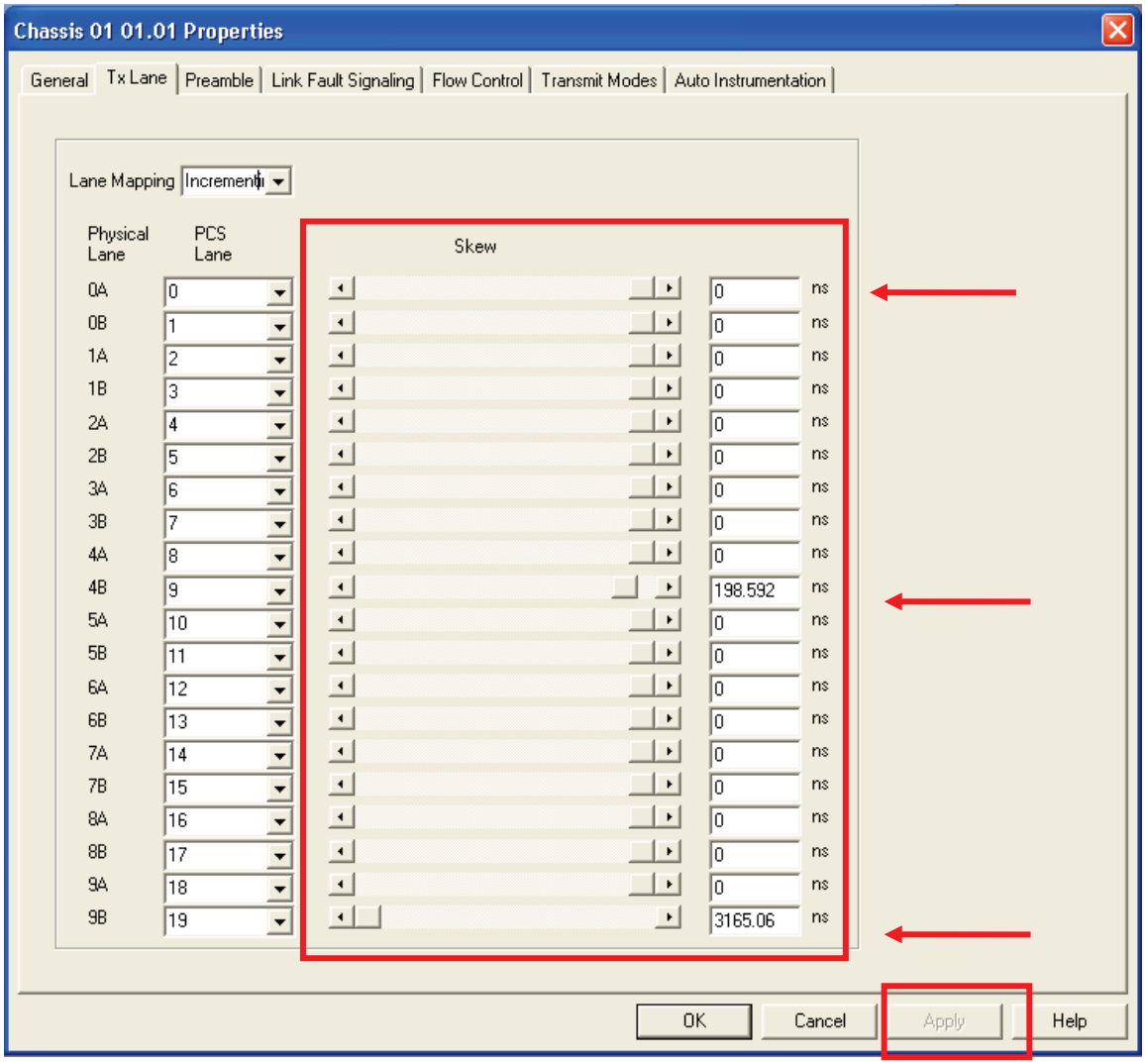
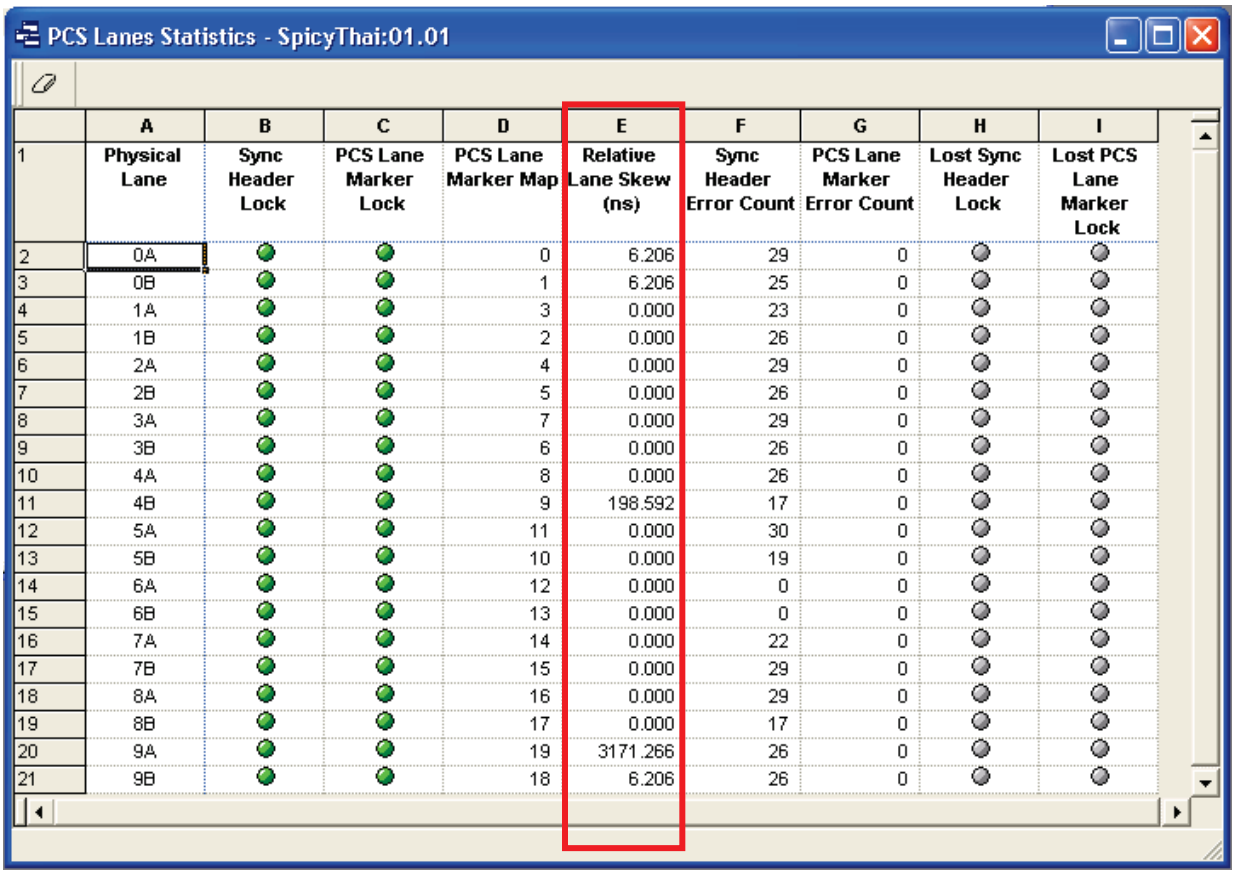


Figure 38. Range of transmit lane skew insertion into the PCS Lanes

4. Next, access the Rx-side of the **PCS Lanes Statistics** dialog box as shown in Figure 39.

5. The Rx-side immediately maps the lanes and measures lane skew while keeping the link up. Reference Figure 39.



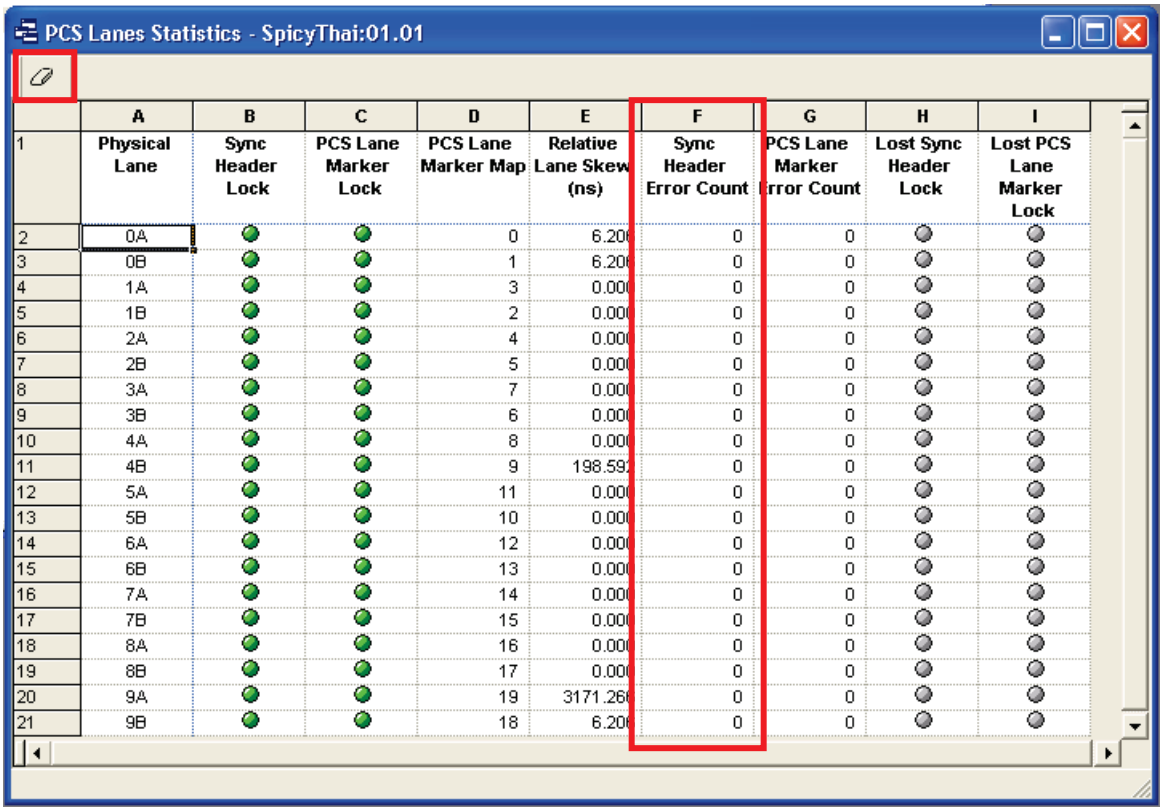
	A	B	C	D	E	F	G	H	I
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			0	6.206	29	0		
3	0B			1	6.206	25	0		
4	1A			3	0.000	23	0		
5	1B			2	0.000	26	0		
6	2A			4	0.000	29	0		
7	2B			5	0.000	26	0		
8	3A			7	0.000	29	0		
9	3B			6	0.000	26	0		
10	4A			8	0.000	26	0		
11	4B			9	198.592	17	0		
12	5A			11	0.000	30	0		
13	5B			10	0.000	19	0		
14	6A			12	0.000	0	0		
15	6B			13	0.000	0	0		
16	7A			14	0.000	22	0		
17	7B			15	0.000	29	0		
18	8A			16	0.000	29	0		
19	8B			17	0.000	17	0		
20	9A			19	3171.266	26	0		
21	9B			18	6.206	26	0		

Figure 39. Example of the range of measured transmit lane skew*

Note. The PCS Lanes Statistics Rx-side can measure up to 6 microseconds of lane skew. The upper limit for the transmit skew insertion is 3 microseconds from the Ixia 40Gb/s and 100Gb/s test system.

6. To remove the errors from the Rx-side PCS Lanes Statistics, click on the clear statistics icon as shown in Figure 40. The **Sync Header Error Count** values are all reset to zero. Notice that the lane skew is not cleared.

   The skew that is injected from the Tx-side will remain on the link until the **Tx Lane** dialog box is reset to a skew value of zero and re-applied. This will set the skew back to zero as seen from the Rx-side PCS Lanes dialog box.



	A	B	C	D	E	F	G	H	I
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			0	6.20	0	0		
3	0B			1	6.20	0	0		
4	1A			3	0.00	0	0		
5	1B			2	0.00	0	0		
6	2A			4	0.00	0	0		
7	2B			5	0.00	0	0		
8	3A			7	0.00	0	0		
9	3B			6	0.00	0	0		
10	4A			8	0.00	0	0		
11	4B			9	198.59	0	0		
12	5A			11	0.00	0	0		
13	5B			10	0.00	0	0		
14	6A			12	0.00	0	0		
15	6B			13	0.00	0	0		
16	7A			14	0.00	0	0		
17	7B			15	0.00	0	0		
18	8A			16	0.00	0	0		
19	8B			17	0.00	0	0		
20	9A			19	3171.26	0	0		
21	9B			18	6.20	0	0		

Figure 40. Example of the range of measured transmit lane skew with the errors removed

Results Analysis

The Rx-side of the PCS Lanes Statistics dialog box shows the skew for each PCS lane that was transmitted to it. All of the measurements are within two clock periods (i.e. 12.412 nanoseconds) or less, compared to the amount of lane skew injected from the transmit port.

Physical Lane 9 shows the maximum amount of skew insertion which is 3,171.266 nanoseconds of lane skew. The minimum is 0 nanoseconds.

Notice that all the LED indicators, columns **B**,**C**, **G**, and **H** are lit green or gray, as they should be for a healthy HSE link.

There were no errors detected in the **PCS Lane Marker Error Count** column. This means that each lane transmitted correctly over its assigned physical lane.

The errors that are seen in the **Sync Header Error Count** column show how many PCS Lane 64B 66B encoded block bit-synchronization errors occurred during the time when the lane skew was applied plus the time required to restore the link. These errors are expected because there were different arrival times at the Rx-side across all of the lanes. This caused varying synchronization time frames per lane, to re-synchronize and restore the link. The delays that the RX-side sees reflect the number of 64B/66B errors Ixia measured as it maintained the 100 Gb/s link.

Test Case: PCS Lane Transmit Error Injection and Receive Measurement Analysis

Per the IEEE802.3ba, section 82.2.8, two bit-interleaved parity (BIP) fields (BIP_3 and BIP_7)are added to each PCS Lane alignment marker. This allows accurate and fast determination of the bit error ratio for a given PCS Lane. This information is used to update bit error counters that the Ixia records in real time. The error measurements are also presented in real time. Users can quickly and easily begin injecting errors into the PCS Lanes mechanism to test their product's design and compliance to the IEEE standard.

Ixia's 40 and 100 Gb/s test system with the IxExplorer GUI allows the user to perform negative tests by injecting bit-level errors into the transmit PCS. The errors may be input in hexadecimal or in binary format in pre-defined fields. The deliberate injection of bit errors into the PCS lane marker provides an excellent mechanism to test the receive PCS (Rx-side) ability to detect these errors and recover the link. This type of testing is intended to validate the correct operation of the PCS RX-side per the IEEE 802.3ba standard.

The user has access to the fields of the alignment marker and 66 bit encoded word payload as shown below:

- Lane Markers
    - Sync bit field for the alignment marker
    - Lane Marker M0, M1, M2 fields
    - BIP3 field
    - Lane Marker M4, M5, M6 fields
    - BIP7 field
    - Field entries can be made in HEX or binary formats
- Lane Markers and Payload
    - Sync bit field for the alignment marker
    - HEX entry for the alignment marker
    - Sync bit field for the 66 bit encoded word
    - Byte 0 through byte 7 of the 66 bit encoded word

  - Field entries for the lane marker are in HEX
  - Field entries for the 66-bit encoded word are in binary

The controls available are designed to do the following:

- Lane Markers
  - Define the PCS Lane to inject one or more errors
  - Determine the number of periods that the errors will be generated for the lane marker
  - Enter a value for a count of consecutive errors to be generated
  - How many times to repeat the periods, or to continuously send the errors as defined by the other controls

Accessing the BIP PCS Lane Error Generation Dialog Screens

Accessing the PCS Lane Error Generation dialog box

To open the PCS Lane Error Generation dialog box:

1. Select the load module in the left pane of the IxExplorer window.
2. Select the port of the load module where the test will be executed.
3. Select the **PCS Lane Error Generation** in the right hand pane of the IxExplorer window.
4. Double-click the **PCS Lane Error Generation**. This opens the PCS Lane Error Generation dialog box.

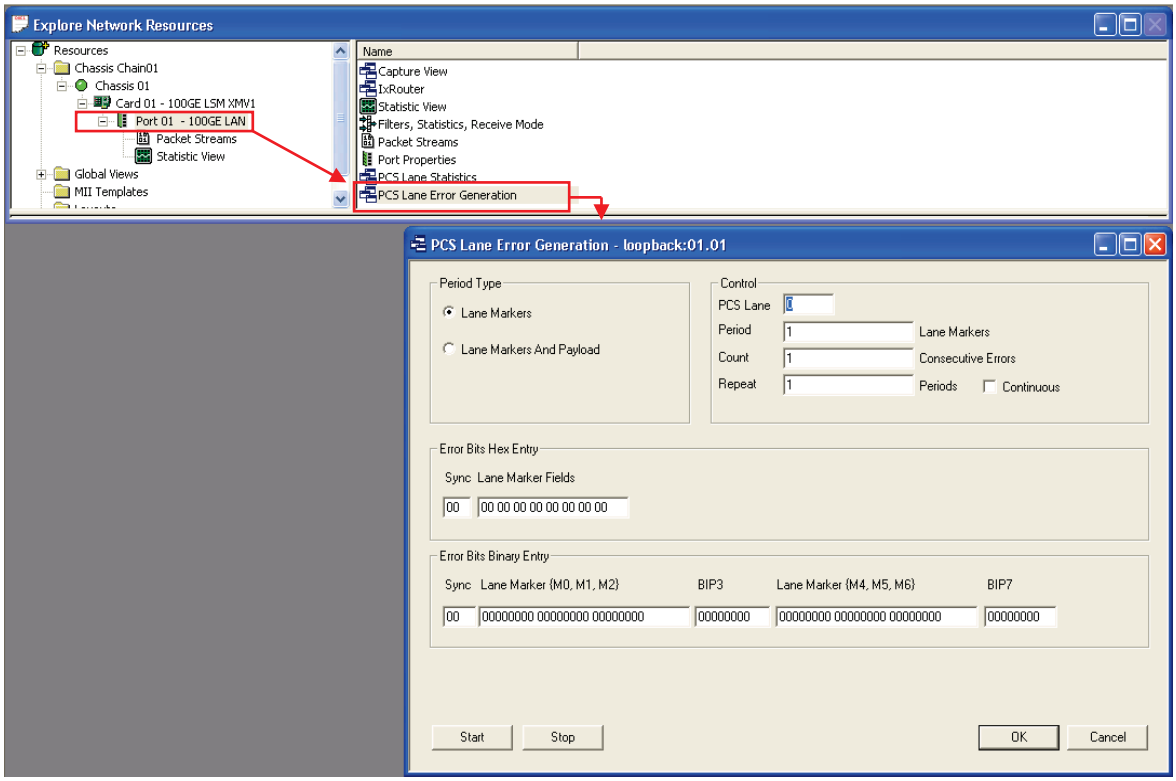


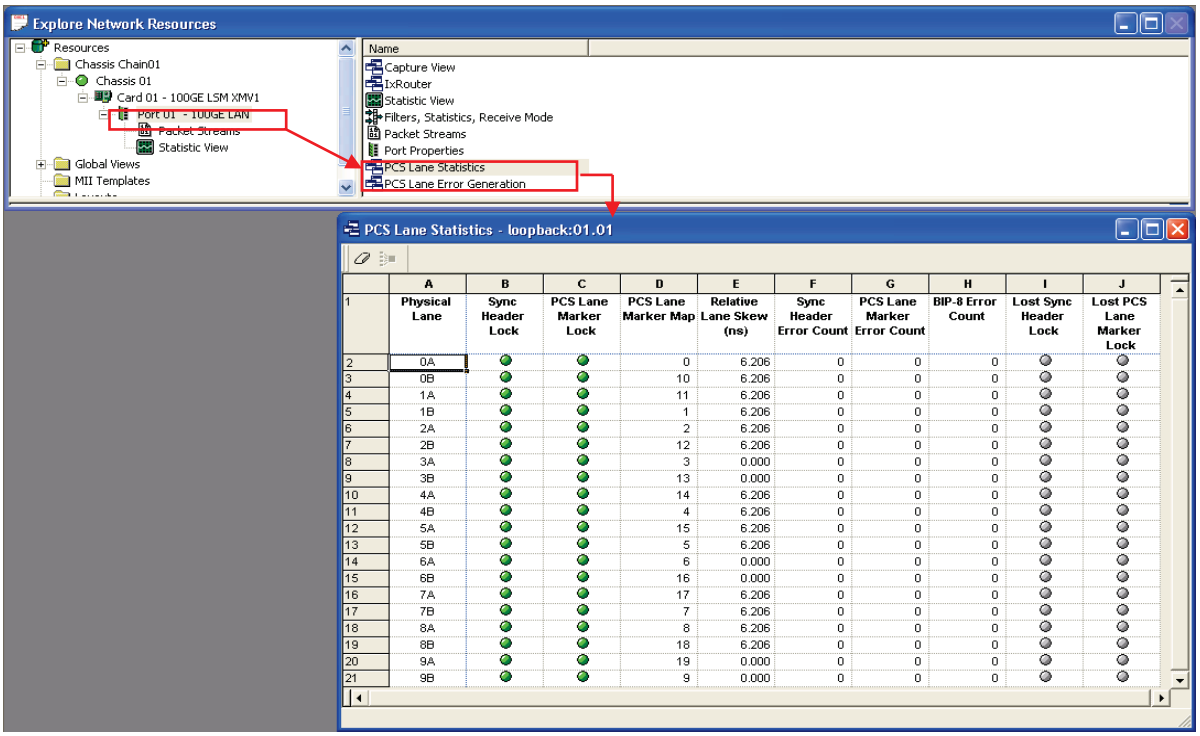
Figure 41. How to access the PCS Lane Error Generation control fields

When testing BIP3 and 7, PCS lane alignment markers and encoded payload blocks the PCS Lane Error Generation dialog box is the transmit side (Tx-Side) of the test, and the PCS Lane Statistics dialog box is the receive side (Rx-Side) of the test.

Accessing the PCS Lane Statistics dialog box

To open the **PCS Lane Statistics** dialog box:

1. Select the load module in the left pane of the IxExplorer window.
2. Select the port of the load module where the test will be executed.
3. Select the **PCS Lane Statistics** in the right hand pane of the IxExplorer window.
4. Double-click the **PCS Lane Statistics**. This opens the PCS Lane Statistics dialog box.



	A	B	C	D	E	F	G	H	I	J
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	BIP-8 Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			0	6.206	0	0	0		
3	0B			10	6.206	0	0	0		
4	1A			11	6.206	0	0	0		
5	1B			1	6.206	0	0	0		
6	2A			2	6.206	0	0	0		
7	2B			12	6.206	0	0	0		
8	3A			3	0.000	0	0	0		
9	3B			13	0.000	0	0	0		
10	4A			14	6.206	0	0	0		
11	4B			4	6.206	0	0	0		
12	5A			15	6.206	0	0	0		
13	5B			5	6.206	0	0	0		
14	6A			6	0.000	0	0	0		
15	6B			16	0.000	0	0	0		
16	7A			17	6.206	0	0	0		
17	7B			7	6.206	0	0	0		
18	8A			8	6.206	0	0	0		
19	8B			18	6.206	0	0	0		
20	9A			19	0.000	0	0	0		
21	9B			9	0.000	0	0	0		

Figure 42. How to access the PCS Lane Statistics measurements window

Both of these screens can be opened in the GUI so that it is easy to switch between them when first using the dialog boxes to gain familiarity.

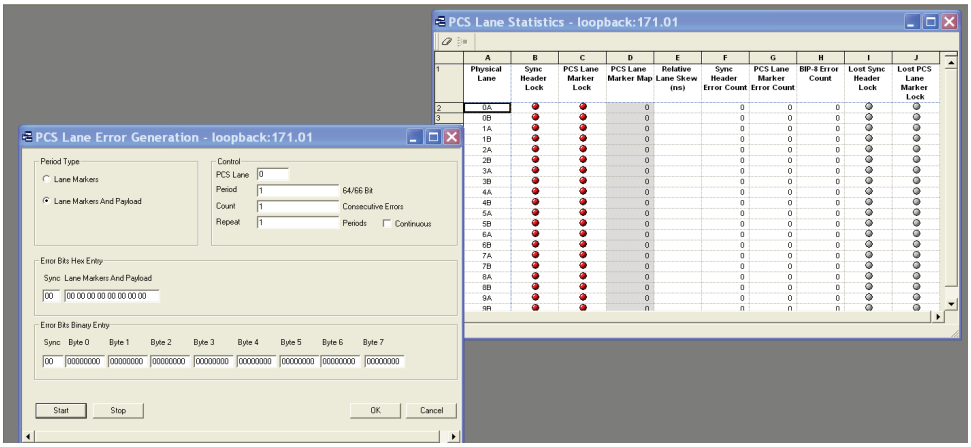


Figure 43. Working view of PCS Lane Error Generation and Lane Statistics dialog boxes

There are two modes, called Period Types to work within the PCS Lane Error Generation dialog box: Lane Markers and, Lane Markers and Payload. The Control field and the Error Bits Binary Entry field change when Lane Markers and Payload is selected.

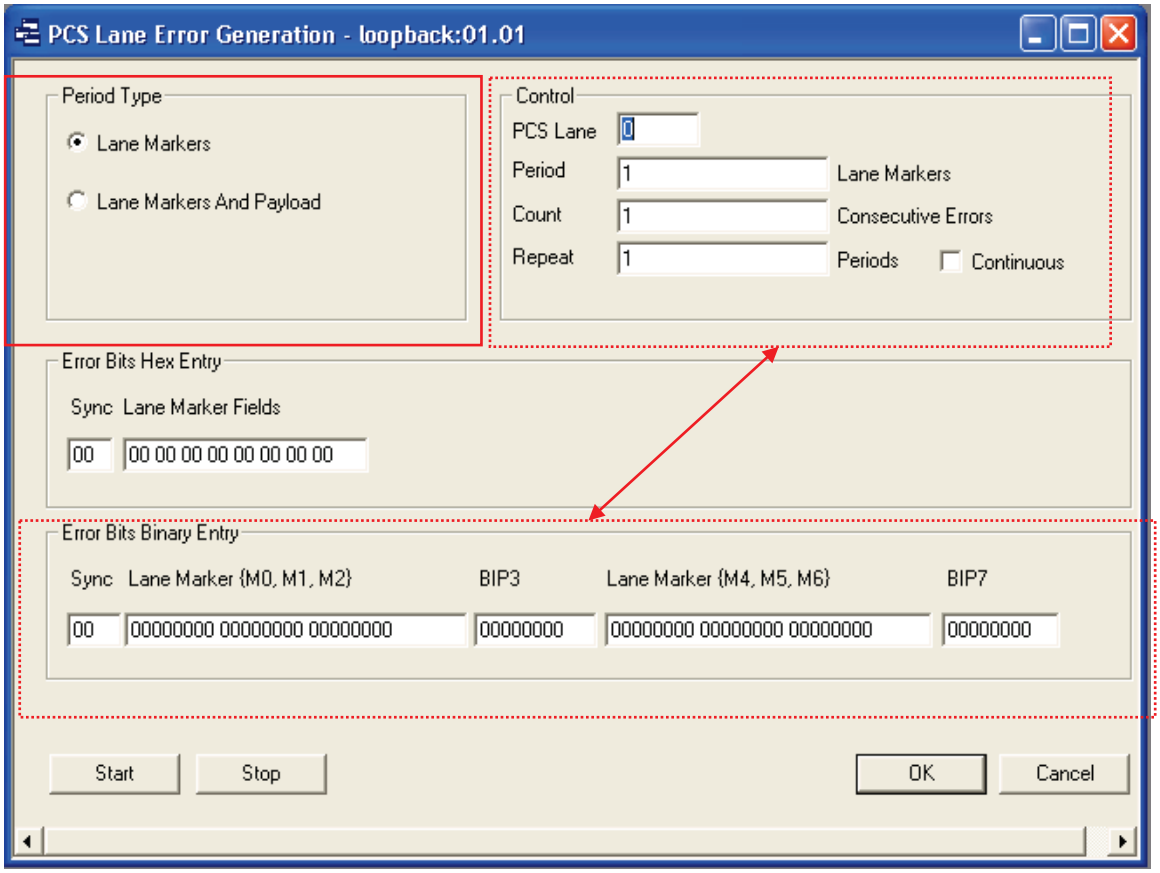


Figure 44. PCS Lane Error Generation screen when Lane Markers is selected. The Red dotted boxes show what fields change when Lane Markers and Payload Period Type is selected

When the Lane Marker Period Type is selected the testing focuses on the specific fields of the lane alignment market including; the synchronization bits, lane marker number bits, the BIP-3 field and the bit-wise inverted fields. Both Period Types in the Ixia GUI presentation represent the design elements of the IEEE 802.3ba standard for these entities. This makes the PCS tests easier to correlate to the standard. Figure 45 is taken directly from the standard. The construction of a lane alignment marker is mimicked in the Ixia PCS Lane Error Generation dialog box (reference Figure 43and Figure 44).

Another fundamental element of injecting bit errors into PCS Lanes is to be clear on the definition of a period on a PCS Lane; the number of 66 bit encoded words between a PCS Lane alignment marker and a subsequent one. Figure 45 is taken right from the IEEE standard. It is important to understand a lane marker period so that the interpretation of bit errors recorded in the BIP3 field of the marker and understanding the correct counting of errors under certain configurations of error injection is critical to make the best use of the IXIA PCS Lane Error Generation and PCS Lane Statistics measurement systems.

The format of the alignment markers is shown in Figure 82–9.

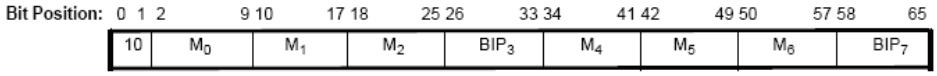


Figure 82–9—Alignment marker format

Figure 45. Source: Draft Amendment to IEEE Std 802.3-2008 IEEE Draft P802.3ba/D2.2, IEEE 802.3ba 40 Gb/s and 100 Gb/s Ethernet Task Force, Aug 15, 2009

The following is paraphrased from the IEEE standard to clarify the definition of a lane alignment market period including when and where they occur on each PCS lane.

82.2.7 Alignment marker insertion

To support deskew and reordering of individual PCS lanes at the receive PCS, alignment markers are added periodically to each PCS lane. The alignment marker has the form of a specially defined 66-bit block with a control block sync header. They interrupt any transfer that is already occurring so that the alignment markers can be inserted into all PCS lanes at the same time. Room for the alignment markers is created by periodically deleting IPG from the XLGMII/CGMII data stream. Other special properties of the alignment markers are that they are not scrambled. This is possible because the alignment markers are added after encoding is performed in the transmit PCS and the alignment markers are removed before decoding is performed in the receive PCS.

The alignment markers are not scrambled in order to allow the receiver to find the alignment markers and re-align all of the data before descrambling is performed. The alignment markers themselves are formed from a known pattern that is defined to be balanced and with many transitions and therefore scrambling is not necessary for the alignment markers. The alignment markers shall be inserted after every 16383 66-bit blocks on each PCS lane.

Figure 46 shows the relationship of PCS Lanes, 66 bit encoded blocks and lane alignment markers.

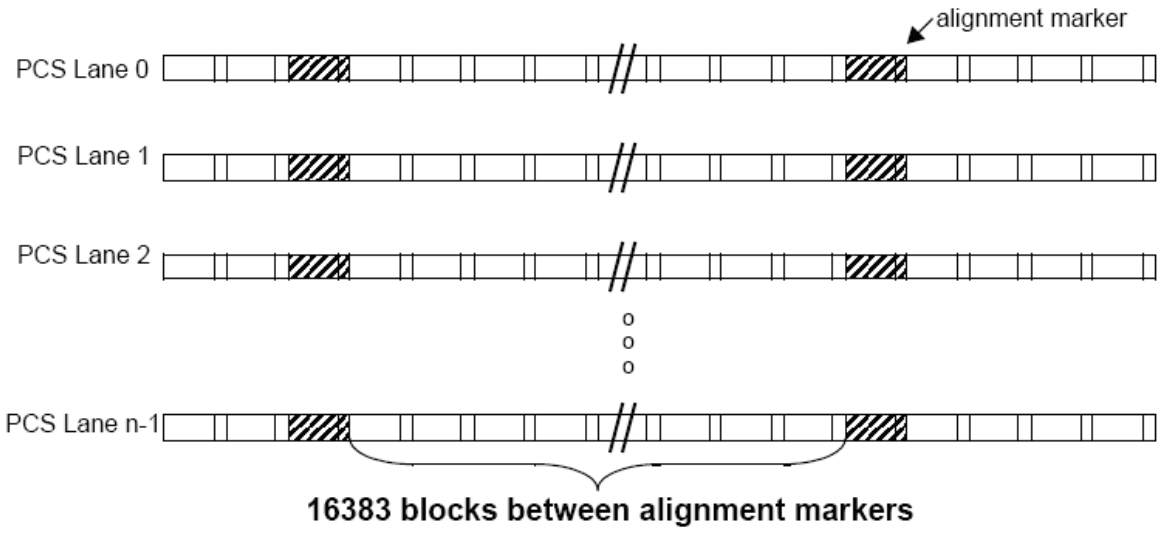


Figure 46. PCS Lane alignment marker insertion period. Source: Draft Amendment to IEEE Std 802.3-2008 IEEE Draft P802.3ba/D2.2, IEEE 802.3ba 40 Gb/s and 100 Gb/s Ethernet Task Force, Aug 15, 2009

In Figure 47, the field changes can be seen when the Lane Markers and Payload Period Type is selected. The changed areas are highlighted in the red outline boxes. When Lane Markers and Payload is selected the test only applies to 64/66 bit encoded words (i.e. data payloads).

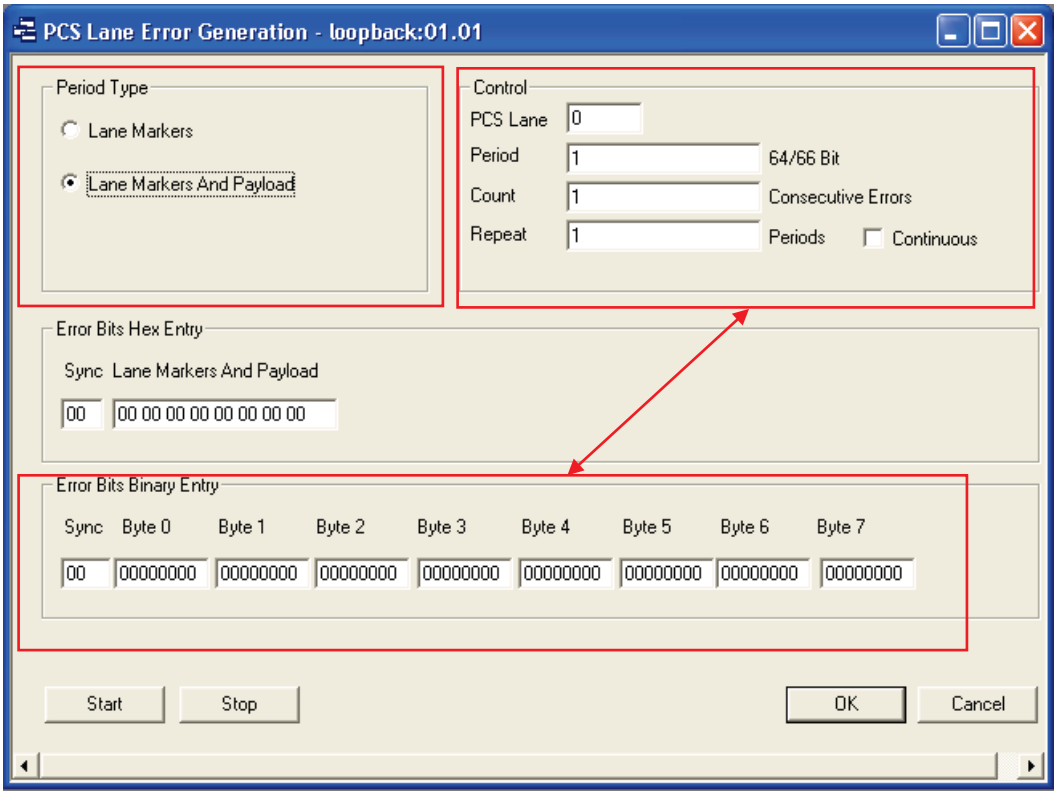


Figure 47. PCS Lane Error Generation dialog box display when Lane Markets and Payload Period Type is selected

Table 8 is provided as a quick reference of the functionality of the IXIA PCS Lane Error Generation error injection system.

Table 8. Summary of PCS Lane Error Generation for Lane Markers and Lane Markers and Payload selections

Section	Field	Description
Period Types	Lane Markers	Insert errors only in the Lane Marker fields.
	Lane Markers and Payload	Insert errors in both Lane Markers and Payload fields.
Control	PCS Lane	Specify which lane to insert errors. 0-19 for 100GBASE-R and 0-3 for 40GBASE-R interface types.
	Period	Define the period by the number of consecutive Lane Markers or 64/66 bit words (depending on Period Type).

Section	Field	Description
	Count	Define the number of consecutive Lane Markers or 64/66 bit Words containing defined errors.
	Repeat	Define the number of periods to repeat any error pattern. Continuous (checkbox) – if selected, the Repeat __ Periods field is disabled, and errors are inserted continuously, or until the STOP button is selected.
Error Bits Hex Entry	Sync /Lane Marker Fields (or) Lane Markers and Payloads	Defines which bits to error, in hex format.
Error Bits Binary Entry		Defines which bits to error, in binary format. Depending on the selected Period Type, the Error Bits Binary Entry units change, either Lane Marker fields or 64/66 bit words.
	If Lane Markers is selected as Period Type	Sync Lane Marker (M0, M1, M2) BIP 3 Lane Marker (M4, M5, M6) BIP 7
	If Lane Markers and Payload is selected as Period Type	Sync and Byte 0 through Byte 7

The last fundamental to understand regarding the PCS Error Generation system is that it is a collection of fields that act as bit or byte masks that overlays a known good 40GBASE-R or 100GBASE-R traffic generation system. Making changes to the fields and controls creates bit errors in predefined, un-errored transmit patterns on the IXIA test system. Changing even one bit in any field can generate one or more errors depending upon exactly which bit was deliberately injected as a transmit error. It is worthwhile to review Clause 82, Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R interfaces to familiarize oneself with the concepts behind the actual operation of the PCS. Knowing when and why bit error measurements and counts occur under particular error situations follows the rules in Clause 82.

The next section has a set of straightforward test cases that are intended to show how to use the most important parts of Ixia PCS Error Generation system. The results are kept simple to demonstrate the basic measurement capabilities of the PCS Lane Statistics menu. Once one is familiar with the power of the Ixia test system, it becomes readily apparent how extreme, in-depth tests can be easily performed. The Ixia test system provides invaluable information to development teams implementing of the new

40GBASE-R and 100GBASE-R PCS systems and how well their products comply with the standard.

Test Case: Injecting a Synchronization Error in a PCS Lane Alignment Marker

Overview

The first test case will inject an error into the synchronization (sync) field by changing one bit in this field.

Objective

This test case causes a sync bit error in the transmission of a PCS lane alignment marker for lane 0. The measurement results will be reviewed.

Step by Step Instructions

1. Access the **PCS Error Generation** dialog box as shown in Figure 41. Refer to the **Accessing the PCS Lane Error Generation dialog box instructions** in the sub-section preceding Figure 42.

2. Select the **Period Type** as **Lane Markers** using the radio button as shown in Figure 48.

3. Change the rightmost bit in the **Sync** field of the **Error Bits Binary Entry** section from a value of 0 to a value of 1. Note the dotted line highlight box that shows an optional way to change the rightmost bit in the **Error Bits Hex Entry** section. A change to one of the two sync fields (Hex or Binary entry) automatically changes the other **Sync** field.

4. The Control field will remain with its default values and when the Sync error is injected it will be on a PCS Lane 0 alignment marker. The error will only last for one period, and only occur once.

5. Press the **Start** button as shown in Figure 48. This will cause the next alignment marker on PCS Lane 0 to be transmitted by the Ixia test system to have a sync error in the marker.

   Note: The error bits set by the user may be sent at any time using the **Start** button. When the **Control** section is using its default values. There is no reason to press the **OK** button to generate the error. Once the **Start** button is pressed the error is generated in real time. Further, injecting the errors can be done when there is the transmission of traffic over the link or when it is idle. The **Stop** button may be

pressed at any time regardless of the settings in the **Period Type** or **Control** sections.

When the **OK** button is pressed the error will be generated. However the **PCS Lane Error Generation** dialog box will be closed. Once closed it has to be re-accessed from the start.

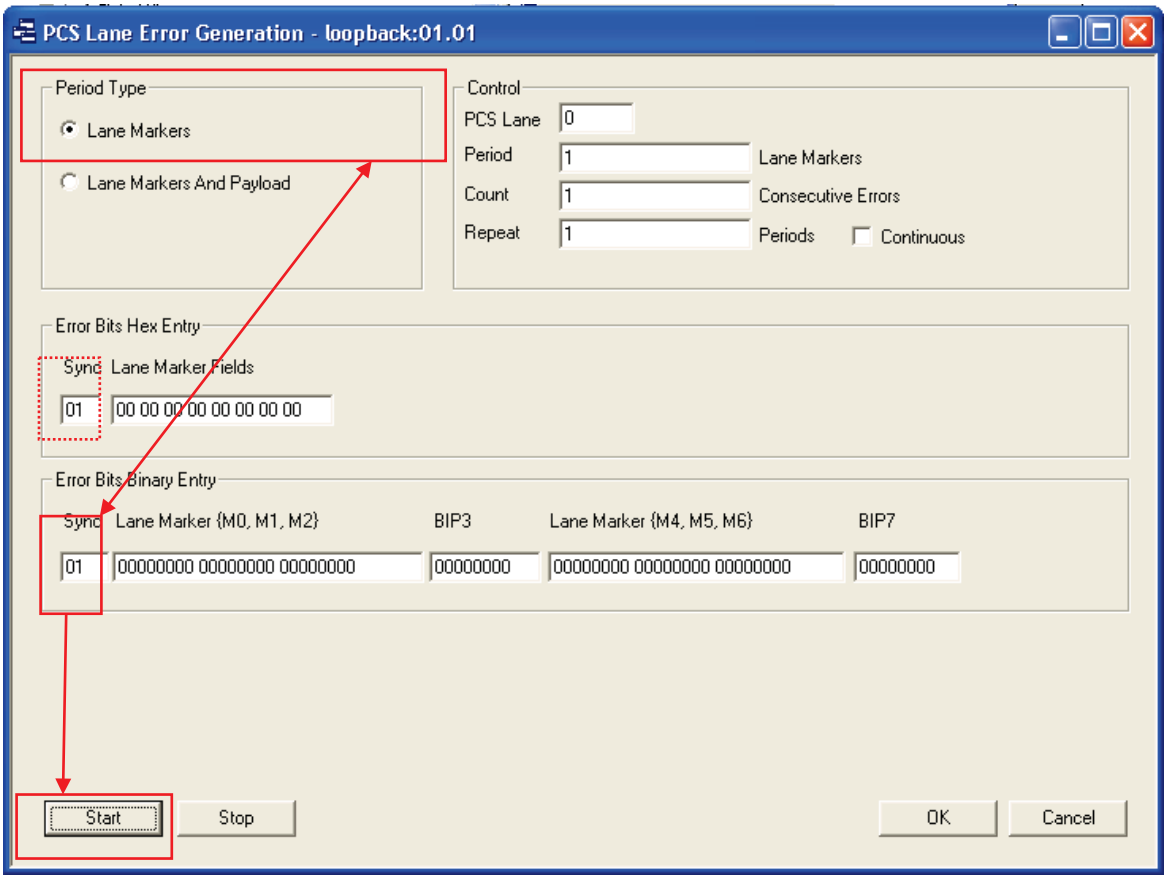


Figure 48. Selecting the Period Type as Lane Markers and injecting a bit error in the Sync field by using the Error Bits Binary Entry section and sending the Sync error by clicking Start

6. Access the **PCS Lane Statistics** dialog box as shown in Figure 42 using the **Accessing the PCS Lane Statistics** dialog box instructions that precede Figure 42. The results of the injection of the sync error in the alignment marker will be shown in the **PCS Lane Statistics** dialog box.

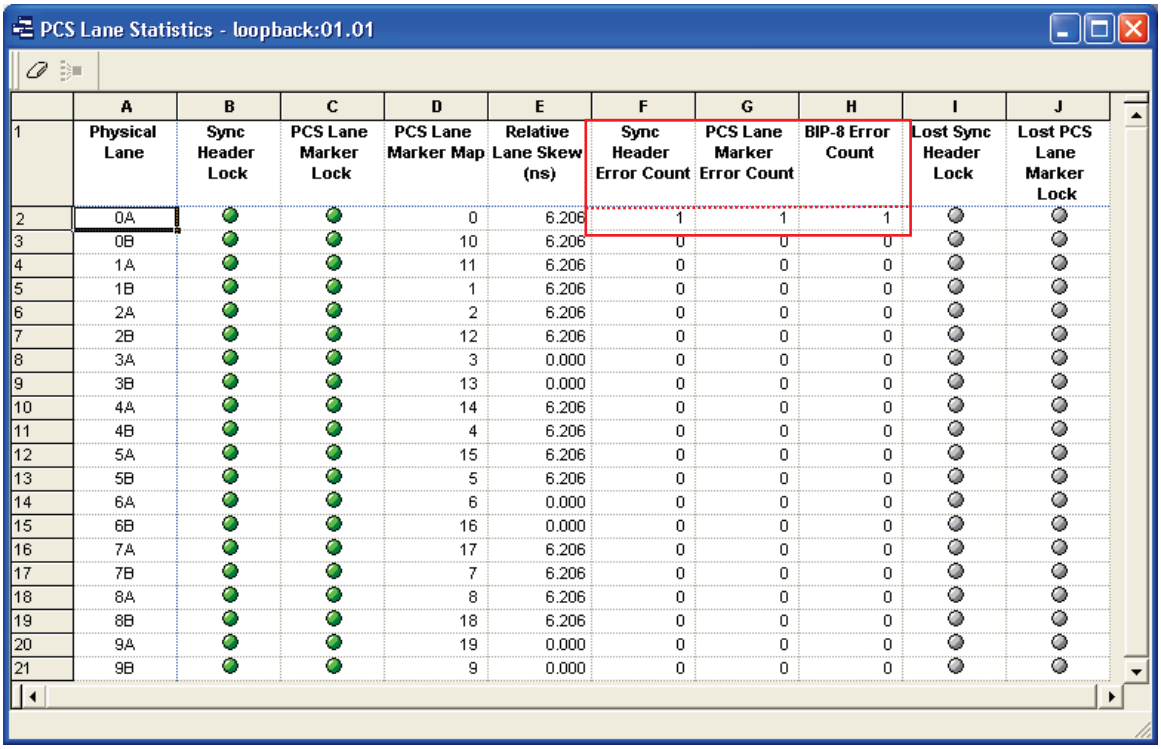
Results Analysis

This is a simple test case. However, an important part of the error tracking in the **PCS Lane Statistics** dialog box is noted. There are three errors counted:

1. A Sync Header Error was detected with a count of 1.
2. A PCS Lane Marker Error was detected with a count of 1.
3. A BIP-8 Error was detected with a count of 1.

A sync error causes three errors. The IEEE802.3ba standard only allows two legal bit patterns in the Sync field: a "01" for an encoded data block and a "10" for a control block, of which an alignment marker always requires a "10" in bit positions 0 and 1 of the Sync field. Any other entry in the Sync field will cause an error.

A lane marker to the PCS system is still a 66-bit word and it follows the same rules with respect to synchronization as other 66 bit words do in the PCS.



	A	B	C	D	E	F	G	H	I	J
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	BIP-8 Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			0	6.206	1	1	1		
3	0B			10	6.206	0	0	0		
4	1A			11	6.206	0	0	0		
5	1B			1	6.206	0	0	0		
6	2A			2	6.206	0	0	0		
7	2B			12	6.206	0	0	0		
8	3A			3	0.000	0	0	0		
9	3B			13	0.000	0	0	0		
10	4A			14	6.206	0	0	0		
11	4B			4	6.206	0	0	0		
12	5A			15	6.206	0	0	0		
13	5B			5	6.206	0	0	0		
14	6A			6	0.000	0	0	0		
15	6B			16	0.000	0	0	0		
16	7A			17	6.206	0	0	0		
17	7B			7	6.206	0	0	0		
18	8A			8	6.206	0	0	0		
19	8B			18	6.206	0	0	0		
20	9A			19	0.000	0	0	0		
21	9B			9	0.000	0	0	0		

Figure 49. Shows results of the sync error injection in the PCS Lane 0 alignment marker's Sync field

It can be seen that the Ixia system recovered the link. All the LED indicators in the **Sync Header Lock** and the **PCS Lane Marker** Lock columns are green. The **PCS Lane Statistics** dialog box will hold the error counts until the user clears them. If the test is run a second time the error counts will accumulate.

Test Case: Injecting a Continuous Sync Error

Overview

The error injection is this test case shows what happens when an error is injected continuously from the Ixia test system.

Objective

This test case will show one of several errors that will bring the link down and the user may see what happens when a continuous error is sent.

Step by Step Instructions

1. Access the **PCS Error Generation** dialog box as shown in Figure 41. Refer to the **Accessing the PCS Lane Error Generation dialog box instructions** in the sub-section preceding Figure 41.
2. Select the **Period Type** as **Lane Markers** using the radio button as shown in Figure 50.
3. Change the rightmost bit in the **Sync** field of the **Error Bits Binary Entry** section from a value of 0 to a value of 1.
4. Go to the **Control** section and set the **Repeat Periods** field to **Continuous** by **check-marking the checkbox** as shown in Figure 49.

5. Press the **Start** button as shown in the following figure. This will cause the next alignment marker and all subsequent PCS Lane alignment markers on PCS Lane 0 to be transmitted by the Ixia test system to have a sync error in the marker.

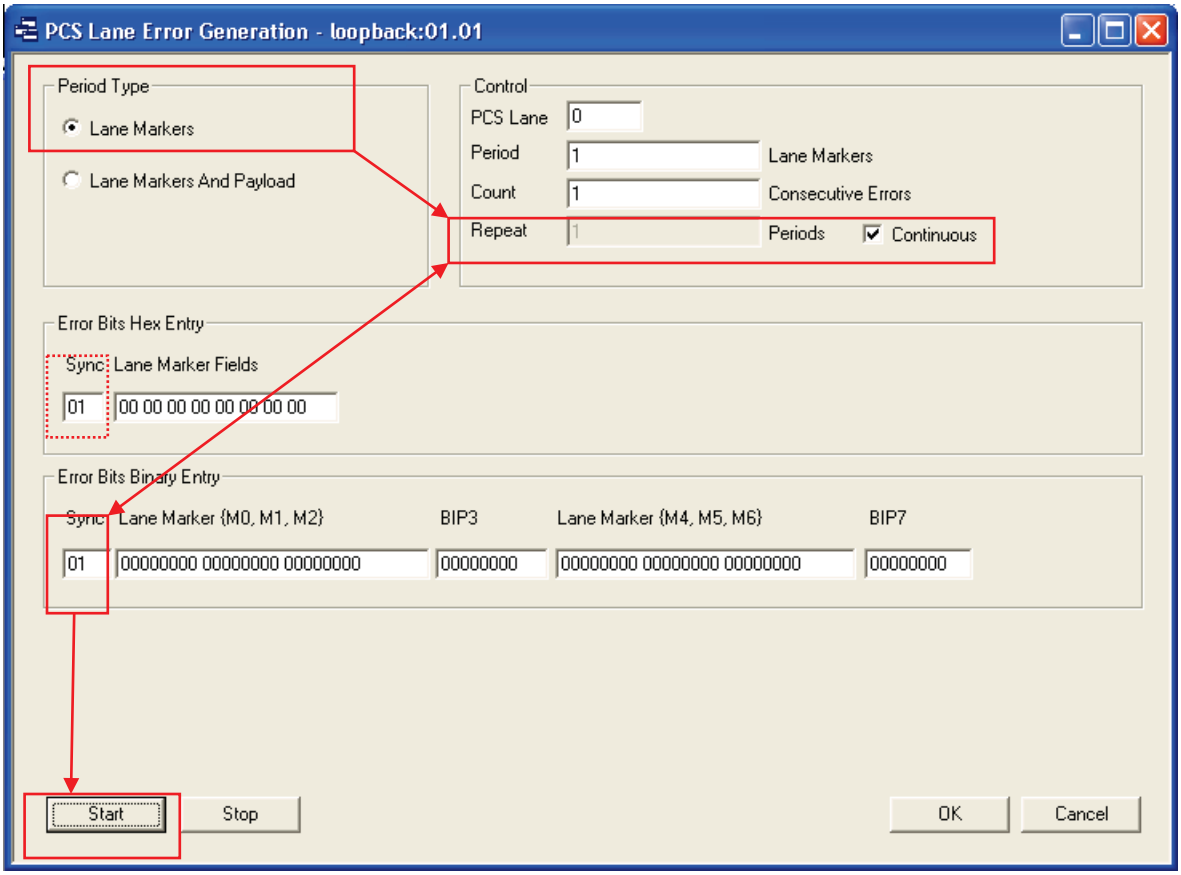


Figure 50. Setting up a continuous error generation of a sync error

Results Analysis

What is seen in Figure 51 is that PCS Lane 0 and its logical lane 0A have these errors

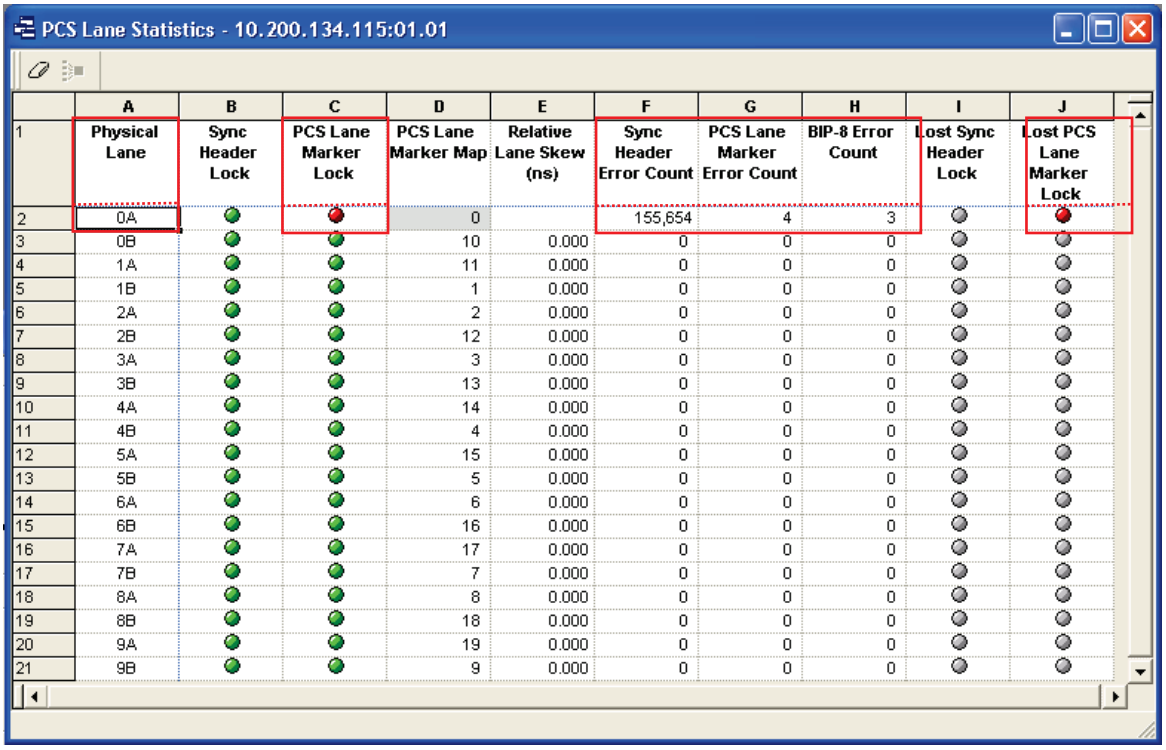
1. **PCS Lane Marker Lock** which is a lack of synchronization beyond all of the link's tolerances for loss of link. The LED indicator is continuously red.

2. There is a very high count of **Sync Header Errors** of 462,434 which would normally continue to accumulate until the Stop button is pressed on the **PCS Error Generation** dialog box. It stopped accumulating counts only because I took a single screen shot capture. What this is really counting is the total number of sync header errors of all the 66 bit words that were received; encoded data and alignment markers.

3. The **PCS LANE Marker Error Count** is 8. This means at the time I took the single screen shot capture that 8 PCS Lane alignment marker periods were missed and counted as errors by the **PCS Lane Statistics** dialog box.

4. The **BIP-8 Error Count** was 3. Here is an interesting behavior of the BIP field. It counts errors in the PCS lane that occur from previous PCS Lane 0 alignment markers, and not in the current one. When the error was set a good alignment marker was sent followed by 4 errored markers, resulting in a count of 3.

5. This time we see that the **Lost PCS Lane Marker Lock** LED indicator went red. This means that since continuous sync errors were sent that the error injection exceeded the tolerance for lane marker loss of synchronization. The rule here is that if the RX-side PCS sees 4 consecutive lane markers with loss of sync, it creates an error condition. Further, once the lane marker sync is lost the Ixia system will continue to accumulate **Sync Header Error Count** numbers because it can no longer identify that markers are coming from PCS Lane 0. Its identification as PCS Lane number 0 is lost from the Rx-side perspective.



	A	B	C	D	E	F	G	H	I	J
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	BIP-8 Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			0		155,654	4	3		
3	0B			10	0.000	0	0	0		
4	1A			11	0.000	0	0	0		
5	1B			1	0.000	0	0	0		
6	2A			2	0.000	0	0	0		
7	2B			12	0.000	0	0	0		
8	3A			3	0.000	0	0	0		
9	3B			13	0.000	0	0	0		
10	4A			14	0.000	0	0	0		
11	4B			4	0.000	0	0	0		
12	5A			15	0.000	0	0	0		
13	5B			5	0.000	0	0	0		
14	6A			6	0.000	0	0	0		
15	6B			16	0.000	0	0	0		
16	7A			17	0.000	0	0	0		
17	7B			7	0.000	0	0	0		
18	8A			8	0.000	0	0	0		
19	8B			18	0.000	0	0	0		
20	9A			19	0.000	0	0	0		
21	9B			9	0.000	0	0	0		

Figure 51. Results of a continuous sync error injection in the PCS Lane 0 in the alignment marker's Sync field

6. Once the **Stop** button is pressed in the PCS Error Generation dialog box, the Ixia 100 GE test system will recover the link so it can continue to test. It is designed to operate in error conditions that would normally be fatal to the link if it were connected to a real network device. If this error occurred on a real 100 GE link

the entire link would go down. The Rx-side of the PCS would not be able to identify PCS Lane 0 and therefore generate many errors and drop the link.

Test Case: Injecting a Lane Marker Error

Overview

This test case example shows how to inject a bit error in just the Lane Marker number identification bytes.

Objective

Demonstrate how to inject only the bytes that report the PCS Lane number and see the behavior of the BIP field.

Step by Step Instructions

1. Access the **PCS Error Generation** dialog box as shown in Figure 41. Refer to the **Accessing the PCS Lane Error Generation dialog box instructions** in the sub-section preceding Figure 41.
2. Select the **Period Type** as **Lane Markers** using the radio button as shown in Figure 52.
3. Change the rightmost bit of the first byte in the **Lane Marker (M0, M1, M2)** field of the **Error Bits Binary Entry** section from a value of 0 to a value of 1.

4. Press the **Start** button as shown in Figure 52. This will cause the next alignment marker on PCS Lane 0 to be transmitted by the Ixia test system to have a bit error in the **Lane Marker**.

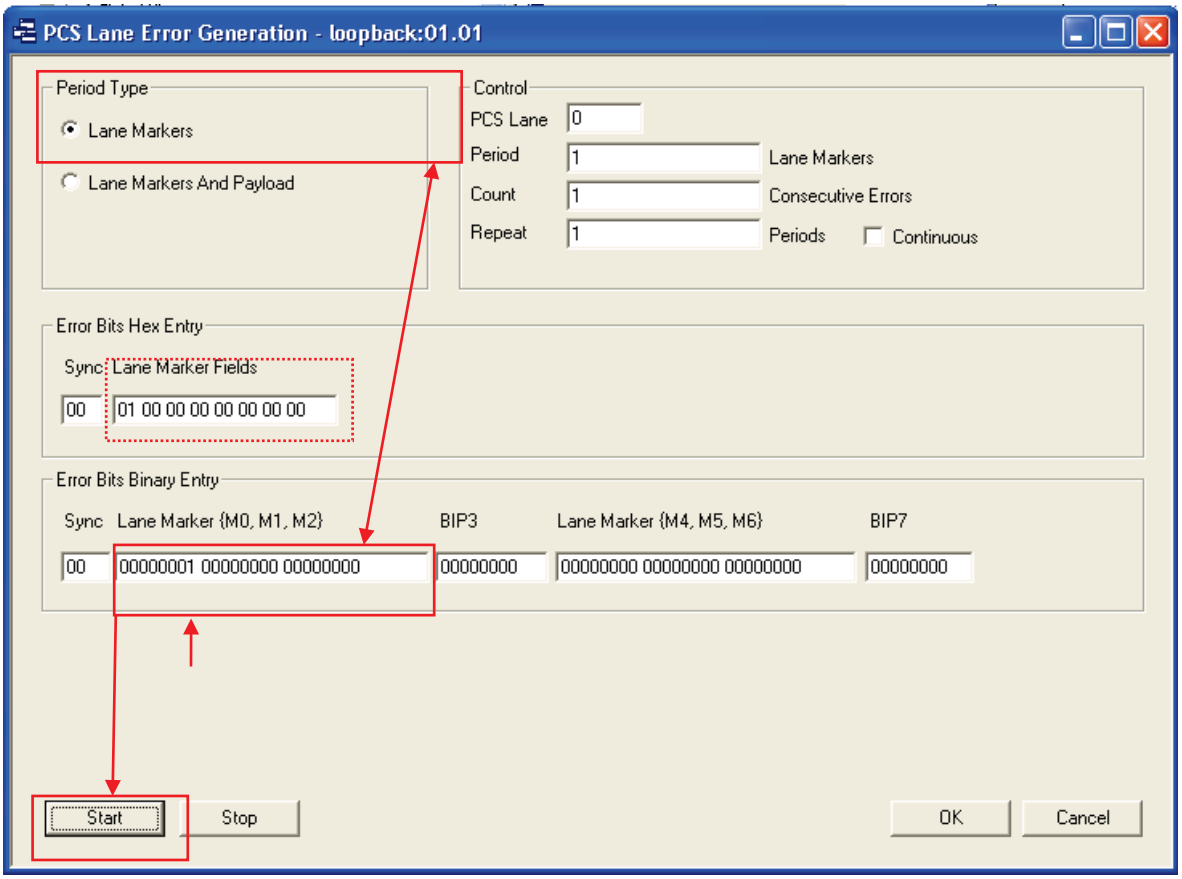
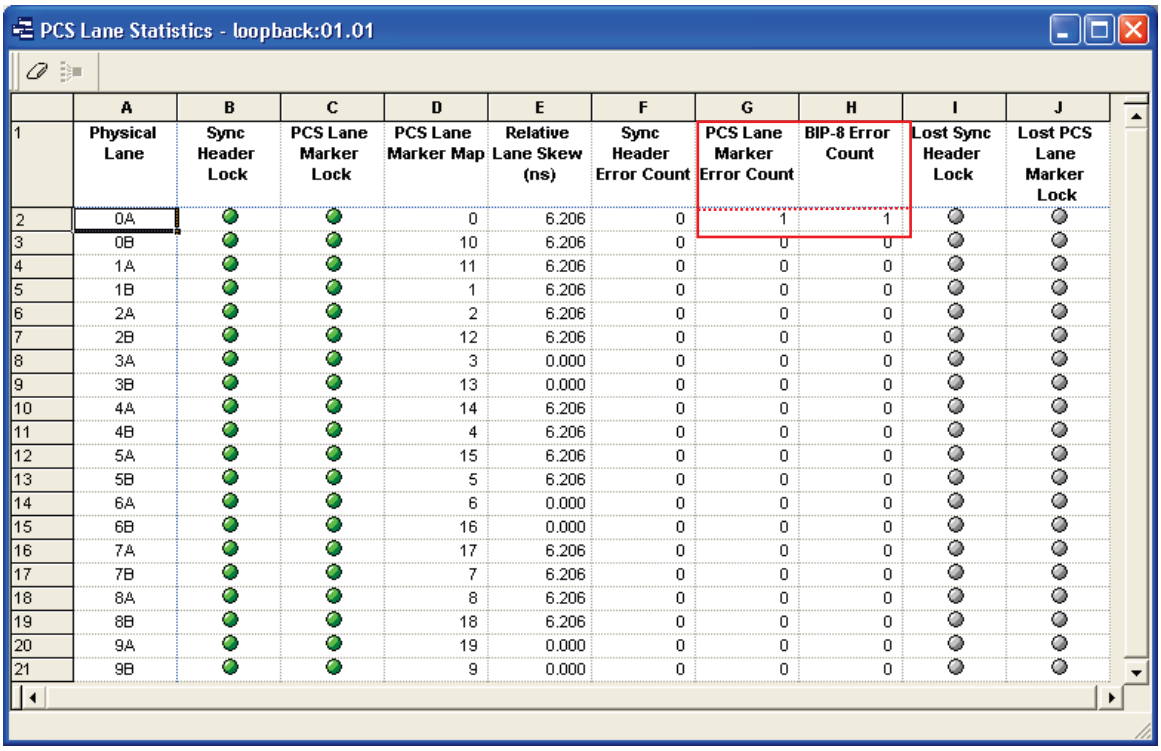


Figure 52. Setting up a bit error in a Lane Marker field

Results Analysis

Byte M0 had a bit error injected. The PCS **Lane Marker Error Count** is 1. The **BIP-8 Error Count** is 1. This is what we should expect as the BIP3 field detects and reports bit errors on the PCS bytes transmitted previous to it.



PCS Lane Statistics - loopback:01.01

	A	B	C	D	E	F	G	H	I	J
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	BIP-8 Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			0	6.206	0	1	1		
3	0B			10	6.206	0	0	0		
4	1A			11	6.206	0	0	0		
5	1B			1	6.206	0	0	0		
6	2A			2	6.206	0	0	0		
7	2B			12	6.206	0	0	0		
8	3A			3	0.000	0	0	0		
9	3B			13	0.000	0	0	0		
10	4A			14	6.206	0	0	0		
11	4B			4	6.206	0	0	0		
12	5A			15	6.206	0	0	0		
13	5B			5	6.206	0	0	0		
14	6A			6	0.000	0	0	0		
15	6B			16	0.000	0	0	0		
16	7A			17	6.206	0	0	0		
17	7B			7	6.206	0	0	0		
18	8A			8	6.206	0	0	0		
19	8B			18	6.206	0	0	0		
20	9A			19	0.000	0	0	0		
21	9B			9	0.000	0	0	0		

Figure 53. The measured results of a single bit error in a Lane Marker field

Test Case: Injecting Multiple Lane Marker Errors

Overview

In this test example, three bytes of the lane marker will have bit errors injected.

Objective

Show how the BIP field counts errors when multiple bytes in a lane marker have bit errors.

Step by Step Instructions

1. Access the **PCS Error Generation** dialog box as shown in Figure 41. Refer to the **Accessing the PCS Lane Error Generation dialog box instructions** in the sub-section preceding Figure 41.
2. Select the **Period Type** as **Lane Markers** using the radio button as shown in Figure 54.
3. Change the value of 0 to a value of 1for the rightmost bit of byte M0, the second bit in Byte M1, and the third bit in Byte M2 in the **Lane Marker (M0, M1, M2)** field of the **Error Bits Binary Entry** section.

4. Press the **Start** button as shown in Figure 54. This will cause the next alignment marker on PCS Lane 0 to be transmitted by the Ixia test system to have multiple bit errors in the **Lane Marker** for PCS Lane 0.

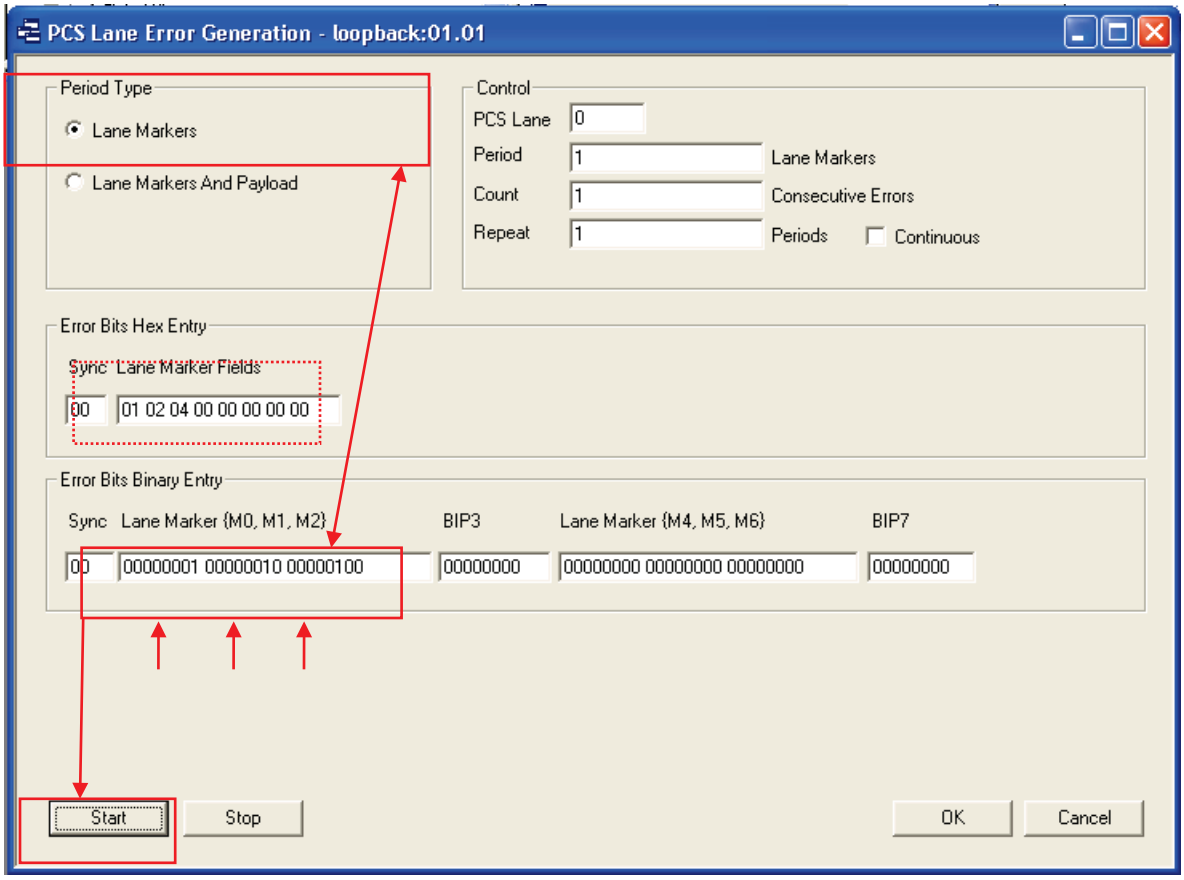
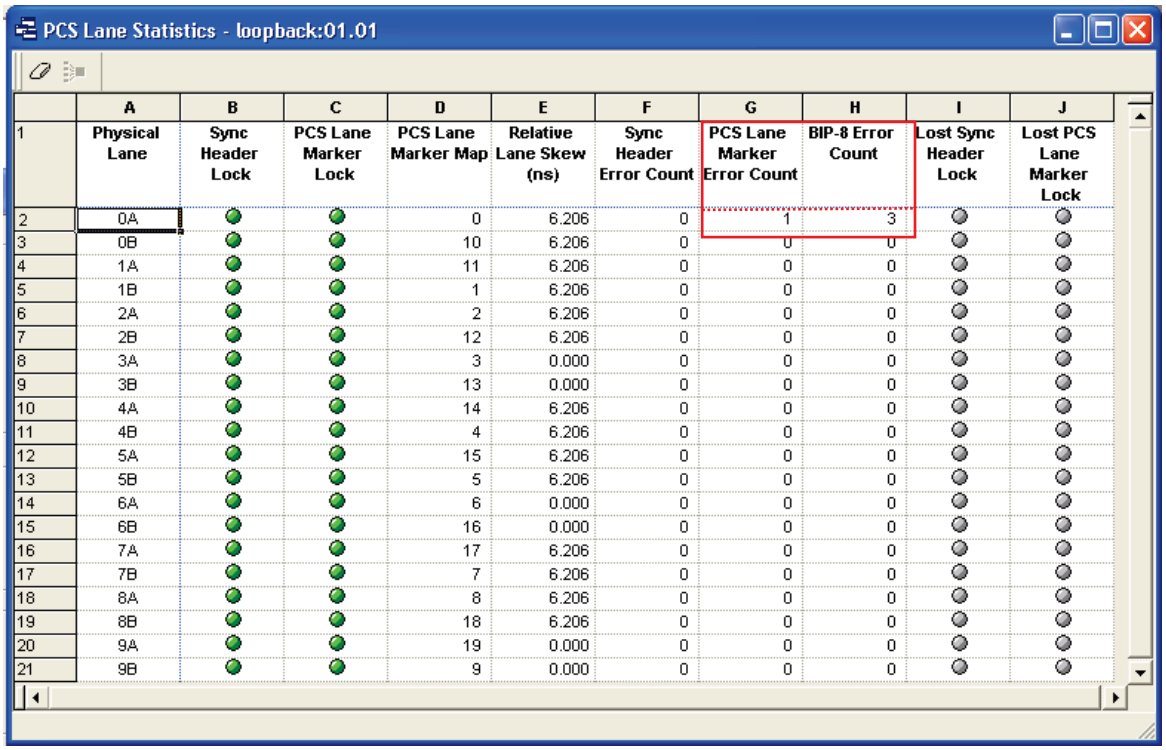


Figure 54. Setting up multiple bit errors in Lane Marker for PCS Lane 0

Results Analysis

The BIP3 field tracks the errors by performing an XOR function over the previous PCS alignment marker bits and all of the previous 16383 66 bit words. In this case, the **Control** field only injected the bit error in each of the three bytes M0, M1, and M2 one time. Because we changed the value from different bit positions in each byte of the Lane Marker number field, the **BIP-8 Error Counter** will be 3. If the bit positions were all changed from 0 to 1 for the same bit position of each of the three bytes M0, M1, and M2, the **BIP-8 Error Counter** would only count 1 error. Because only one alignment marker was sent per the setup in the **Control** section, the count for the PCS lane marker is a count of 1.



	A	B	C	D	E	F	G	H	I	J
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	BIP-8 Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			0	6.206	0	1	3		
3	0B			10	6.206	0	0	0		
4	1A			11	6.206	0	0	0		
5	1B			1	6.206	0	0	0		
6	2A			2	6.206	0	0	0		
7	2B			12	6.206	0	0	0		
8	3A			3	0.000	0	0	0		
9	3B			13	0.000	0	0	0		
10	4A			14	6.206	0	0	0		
11	4B			4	6.206	0	0	0		
12	5A			15	6.206	0	0	0		
13	5B			5	6.206	0	0	0		
14	6A			6	0.000	0	0	0		
15	6B			16	0.000	0	0	0		
16	7A			17	6.206	0	0	0		
17	7B			7	6.206	0	0	0		
18	8A			8	6.206	0	0	0		
19	8B			18	6.206	0	0	0		
20	9A			19	0.000	0	0	0		
21	9B			9	0.000	0	0	0		

Figure 55. The measured results of multiple bit errors in a Lane Marker field of the bytes M0, M1, and M2

Test Case: Injecting Multiple Errors into 66 bit Data Payload Word

Overview

Errors will set up in 66 bit encoded words and the error counting behavior of the BIP field is shown.

Objective

This test will demonstrate using the **Lane Markers and Payload**, **Period Type** selection.

Step by Step Instructions

1. Access the **PCS Error Generation** dialog box as shown in Figure 41. Refer to the **Accessing the PCS Lane Error Generation dialog box instructions** in the sub-section preceding Figure 41.
2. Select the **Period Type** as **Lane Markers And Payload** using the radio button as shown in Figure 56.
3. Change the value of 0 to a value of 1 for the rightmost bit of byte 0, the second bit in Byte 1, the third bit in Byte 2, and the fourth bit in Byte 3 in the **Error Bits Binary Entry** section.

   Note that the **Error Bits Hex Entry** field shows the actual hex value of each byte of the payload with an injected bit error.
4. Press the **Start** button as shown in Figure 56. This will cause an encoded 66 bit word on PCS Lane 0 to be transmitted by the Ixia test system to have multiple bit errors in the **payload bytes of the 66 bit word** for PCS Lane 0.

5. The **Control** section is set up to only error one 66 bit word in one period.

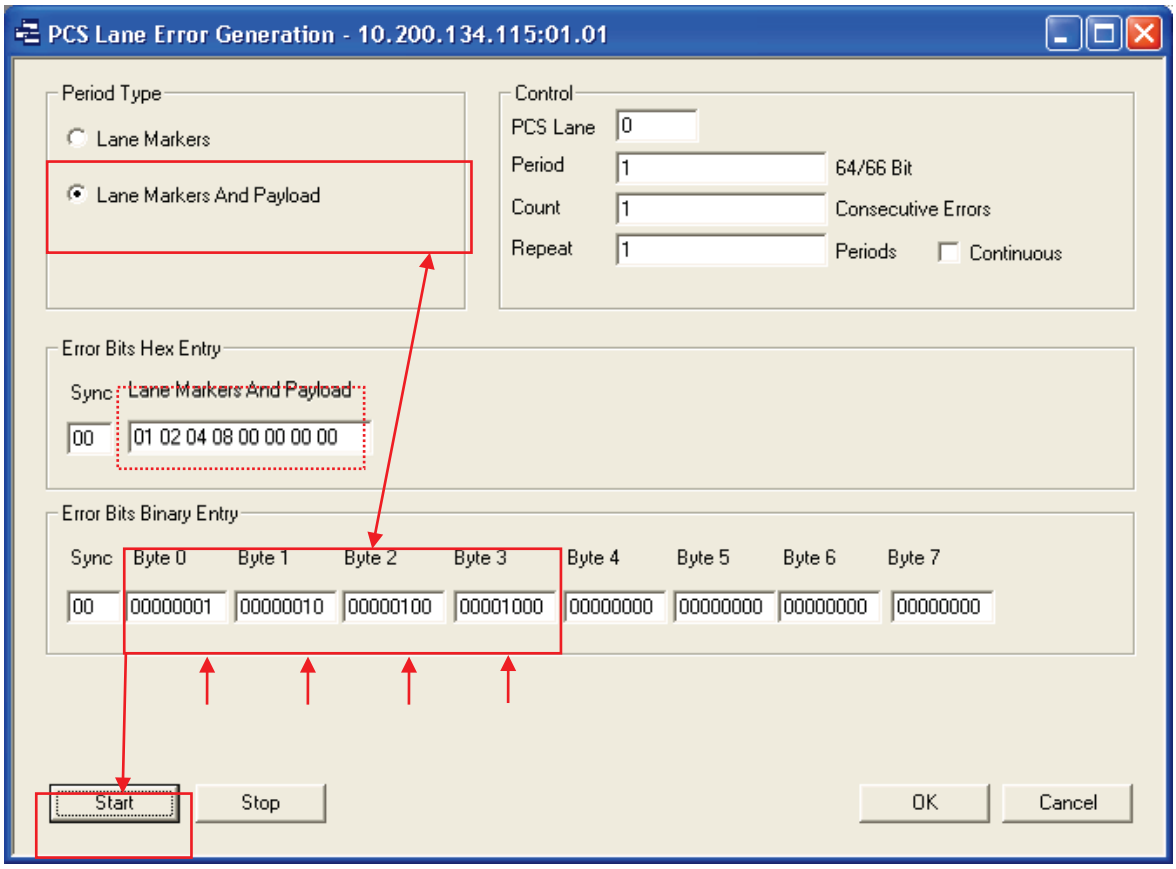
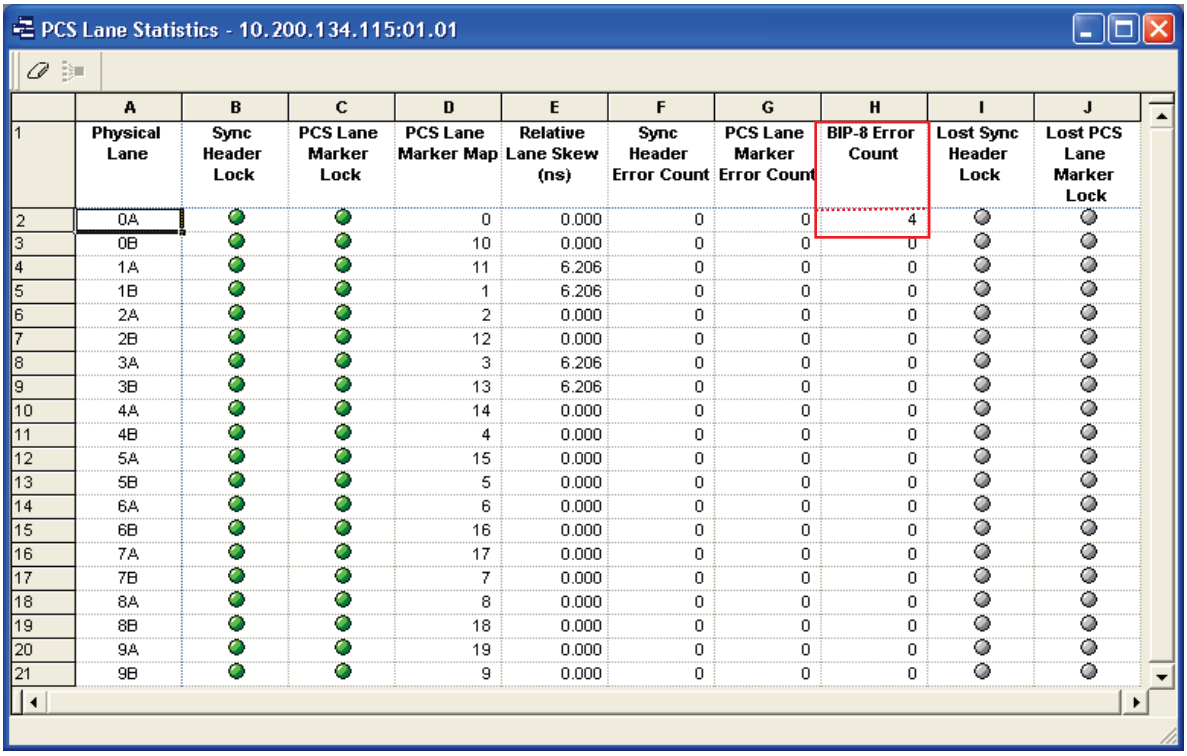


Figure 56. Setting up multiple bit errors by using Lane Markers and Payload Period Type for PCS Lane 0

Results Analysis

The BIP-8 Error Count shows a count of 4 that correlates to the bytes 0 through 3 that were given an error bit. Since there was only one lane alignment marker sent with an error, there is no loss of PCS Lane Marker Loss, or Sync Header Lock, and the link is not dropped.



PCS Lane Statistics - 10.200.134.115:01.01

	A	B	C	D	E	F	G	H	I	J
1	Physical Lane	Sync Header Lock	PCS Lane Marker Lock	PCS Lane Marker Map	Relative Lane Skew (ns)	Sync Header Error Count	PCS Lane Marker Error Count	BIP-8 Error Count	Lost Sync Header Lock	Lost PCS Lane Marker Lock
2	0A			0	0.000	0	0	4		
3	0B			10	0.000	0	0	0		
4	1A			11	6.206	0	0	0		
5	1B			1	6.206	0	0	0		
6	2A			2	0.000	0	0	0		
7	2B			12	0.000	0	0	0		
8	3A			3	6.206	0	0	0		
9	3B			13	6.206	0	0	0		
10	4A			14	0.000	0	0	0		
11	4B			4	0.000	0	0	0		
12	5A			15	0.000	0	0	0		
13	5B			5	0.000	0	0	0		
14	6A			6	0.000	0	0	0		
15	6B			16	0.000	0	0	0		
16	7A			17	0.000	0	0	0		
17	7B			7	0.000	0	0	0		
18	8A			8	0.000	0	0	0		
19	8B			18	0.000	0	0	0		
20	9A			19	0.000	0	0	0		
21	9B			9	0.000	0	0	0		

Figure 57. Multiple bit errors are counted in a 66 bit data payload word for PCS Lane 0 with the Period Type set to Lane Markers and Payload

Summary

The new PCS Layer for the IEEE 802.3ba standard is a critical enabler of the new higher speed Ethernet technology for 40 Gb/s and 100 Gb/s network interfaces and equipment. Without it, there would be less flexibility in the design of optics and the loss of the ability to use today's component technology. The market window to meet the demand for higher speed Ethernet interfaces is right now. The need for increased bandwidth in data center is a key enabler of the next expansion of the Internet. HSE technology has many market drivers that bring Ethernet's economic and ease-of-use benefits to end users who are managing large data centers and Internet exchanges. Most importantly, HSE speeds will help the communications industry deliver more bandwidth-intensive services over the Internet. Early adopters of the HSE technology recognized the need to bring products to market faster to meet customer demands, even prior to the publication of the IEEE 802.3ba standard.

Ixia recognized the need for a working 100 Gb/s and 40 Gb/s test system prior to publication of the IEEE standard. Ixia made a powerful test tool commercially available in the fourth quarter of 2008, well before the ratification of IEEE standard. Ixia's unique PCS layer test capability has been publicly demonstrated. The test methodologies in this booklet provide a quick study of the in-depth functionality and power of these test systems. The Ixia 40 Gb/s and 100 Gb/s products have many more layer-1, 2 and 3 features not described here as well as the ability to run layer 4 through 7 applications. Ixia's ultimate goal is to assist early adopters of HSE technology to develop and test their designs and to reduce their time-to-market while the market is evolving.

Glossary

Abbreviation	Description
10 GbE	Ethernet that runs at 10Gb/s over fiber and copper media, IEEE802.3ae standard and several follow-on standards.
ASIC	Applications Specific Integrated Circuit
BIP	Bit interleaved parity fields that are used in PCS lane alignment markers to record bit errors that may occur over a lane alignment marker period in a given PCS lane.
DUT	Device under Test
FPGA	Field Programmable Gate Array
HSE	Higher Speed Ethernet
IEEE 802.3ba	The IEEE standard that is now ratified for Higher Speed Ethernet.
IP	Internet Protocol
MLD	Multilane Distribution, the new mechanism for the Physical Coding Sublayer of the IEEE802.3ba standard.
MMF	Multimode fiber
MPO	Connector type that is compatible with a multimode fiber optic ribbon cable with 12-parallel fibers.
OTN	Optical Transport Network
PCS	Physical Coding Sublayer of the IEEE802.3ba standard.
PCS Lane	Physical Coding Sublayer definition of the two bit-interleaved streams that are assigned to a single Physical Lane.
Rx, or Rx-side	Receive side perspective of a physical port in a test or for reception of IP traffic.
SMF	Single mode fiber

Abbreviation	Description
SNAP-12	MSA specification for a multimode 850nm short reach transceiver, modified by Avago Technologies to carry 10 lanes of 10Gb/s of traffic per lane for 100 GE application.
SOC	System on a Chip
Tx, or Tx-side	Transmit side perspective of a physical port in a test or for transmission of test or IP traffic

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