Black Book

ixia

Edition 10

Ethernet Synchronization

http://www.ixiacom.com/blackbook

June 2014

Your feedback is welcome

Our goal in the preparation of this Black Book was to create high-value, high-quality content. Your feedback is an important ingredient that will help guide our future books.

If you have any comments regarding how we could improve the quality of this book, or suggestions for topics to be included in future Black Books, please contact us at ProductMgmtBooklets@ixiacom.com.

Your feedback is greatly appreciated!

Contents

How to Read This Book vii
Dear Reader viii
Introduction and Overview 1
Ethernet Synchronization 2
Terminology, Measurement Methods, and Metrics 7
Testing Ethernet Synchronization Protocols 11
Test Case: PTP Scalability by Using IxNetwork 13
Test Case: PTP Scalability by Using IxN2X 27
Test Case: Best Master Clock (BMC) Selection by Using IxNetwork 35
Test Case: Best Master Clock (BMC) Selection by Using IxN2X 49
Test Case: Correction Factor Error by Using IxNetwork 57
Test Case: Correction Factor Error by Using IxN2X 65
Test Case: ESMC Best Reference Port Selection by Using IxNetwork 77
Test Case: ESMC Port Switching by Using IxNetwork 89
Test Case: ESMC Failover (5-Second Rule) by Using IxNetwork 93
ESMC Test Variables 97
Testing Ethernet Synchronization Clock Quality 99
Test Case: G.8261 – Testing Timing over Packet (Ordinary Clocks) 101
G.8262 – Testing Synchronous Ethernet Equipment Clocks 125
Test Case: Wander Generation 127
Test Case: Wander Tolerance 135
Test Case: Wander Transfer 144
Test Case: Jitter Compliance 155
Test Case: Jitter Tolerance 163
Devices and Topologies 173
Test Case: Boundary Clocks - PTP Timestamp Accuracy (Time Error) 173
Test Case: Transparent Clocks – Correction Field Accuracy 181
Test Case: Hybrid SyncE and PTP - SyncE Islands with PTP Connection 185
Test Case: Hybrid SyncE and PTP - SyncE Frequency and PTP Time 191
Contact Ixia 197

How to Read This Book

The book is structured as several standalone sections that discuss test methodologies by type. Every section starts by introducing the reader to relevant information from a technology and testing perspective.

Each test case has the following organization structure:

Overview	Provides background information specific to the test case.
Objective	Describes the goal of the test.
Setup	An illustration of the test configuration highlighting the test ports, simulated elements and other details.
Step-by-Step Instructions	Detailed configuration procedures using Ixia test equipment and applications.
Test Variables	A summary of the key test parameters that affect the test's performance and scale. These can be modified to construct other tests.
Results Analysis	Provides the background useful for test result analysis, explaining the metrics and providing examples of expected results.
Troubleshooting and Diagnostics	Provides guidance on how to troubleshoot common issues.
Conclusions	Summarizes the result of the test.

Typographic Conventions

In this document, the following conventions are used to indicate items that are selected or typed by you:

- **Bold** items are those that you select or click on. It is also used to indicate text found on the current GUI screen.
- *Italicized* items are those that you type into fields.

Dear Reader

Ixia's Black Books include a number of IP and wireless test methodologies that will help you become familiar with new technologies and the key testing issues associated with them.

The Black Books can be considered primers on technology and testing. They include test methodologies that can be used to verify device and system functionality and performance. The methodologies are universally applicable to any test equipment. step-by-step instructions using Ixia's test platform and applications are used to demonstrate the test methodology.

This tenth edition of the black books includes twenty two volumes covering some key technologies and test methodologies:

Volume 1 – Higher Speed Ethernet

Volume 2 – QoS Validation

Volume 3 – Advanced MPLS

Volume 4 – LTE Evolved Packet Core

Volume 5 – Application Delivery

Volume 6 – Voice over IP

Volume 7 – Converged Data Center

Volume 8 – Test Automation

Volume 9 – Converged Network Adapters

Volume 10 – Carrier Ethernet

Volume 11 – Ethernet Synchronization

Volume 12 – IPv6 Transition Technologies

Volume 13 – Video over IP

Volume 14 – Network Security

Volume 15 – MPLS-TP

Volume 16 – Ultra Low Latency (ULL) Testing

Volume 17 – Impairments

Volume 18 – LTE Access

Volume 19 – 802.11ac Wi-Fi Benchmarking

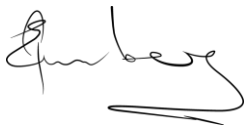
Volume 20 – SDN/OpenFlow

Volume 21 – Network Convergence Testing

Volume 22 – Testing Contact Centers

A soft copy of each of the chapters of the books and the associated test configurations are available on Ixia's Black Book website at http://www.ixiacom.com/blackbook. Registration is required to access this section of the Web site.

At Ixia, we know that the networking industry is constantly moving; we aim to be your technology partner through these ebbs and flows. We hope this Black Book series provides valuable insight into the evolution of our industry as it applies to test and measurement. Keep testing hard.



Errol Ginsberg, Acting CEO

Ethernet Synchronization

Test Methodologies

This document presents a thorough methodology for testing timing and synchronization over packet-based networks. Ethernet synchronization technologies, such as IEEE1588v2 Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) are discussed in depth. Key scenarios describe synchronization protocols and clock quality testing of timing enabled networks and devices.

Introduction and Overview

In this Black Book on testing timing and synchronization over packet networks, Ixia has produced a definitive guide to the technological characteristics of timing and synchronization protocols, and the methodology for testing protocol functionality and synchronization performance of timing enabled network devices.

As network providers roll out the Next Generation Network (NGN), they are looking to extend the life of their existing TDM-based networks to carry IP data and applications seamlessly across Ethernet networks. As transport migrates from TDM networks (SONET, T1, and E1) to packet networks (Ethernet), technologies such as IEEE1588-2008 Precision Timing Protocol (PTP), Circuit Emulation Services (CES), and Synchronous Ethernet (SyncE) are becoming common methods for delivering timing and synchronization throughout the Ethernet network. This is driven by the fact that native Ethernet does not have an embedded timing distribution capability. Synchronous Ethernet allows Ethernet to distribute a clock signal with a highly accurate frequency at the physical layer in a similar manner to the capability that already exists in TDM networks. However, new requirements – such as distributing Time-of-Day (ToD) to meet requirements in the mobile space to achieve phase alignment – cannot be met by Synchronous Ethernet frequency distribution alone. IEEE1588 is able to deliver ToD information in order to enable phase alignment over Ethernet networks. Other applications such as video streaming and interactive gaming may also require accurate ToD distribution.

Network engineers are increasingly developing and deploying IEEE1588 devices such as Transparent Clocks, Boundary Clocks, Master Clocks and Slave Clocks, as well as packet forwarding equipment that use Synchronous Ethernet to distribute frequency synchronization. Further, hybrid networks using a combination of PTP and SyncE are emerging. It is critical for engineers to develop and execute plans for testing the functionality, timing accuracy, performance, and scalability of these devices.

Ethernet Synchronization

Ethernet Synchronization Technology

As the demand for advanced mobile broadband services continues to increase, many network providers and carriers are migrating their mobile backhaul networks from legacy synchronous transports, such as SONET/SDH and T1/E1, to Carrier Ethernet. Traditional TDM networks provided not only data transport, but also synchronization of frequency. Synchronization equivalent to what has been provided for TDM networks must be provided on Ethernet networks for Ethernet to be used as a replacement for TDM. This must be done without impact to the synchronization quality and network performance. In addition, modern wireless networks are demanding time/phase synchronization as well. It is critical to verify synchronization performance of Ethernet network elements before deployment.

Three primary methods are used to deliver synchronization over Ethernet:

- Circuit Emulation Service (CES): TDM frames from T1 or E1 circuits are encapsulated and transported directly over Ethernet, often in pseudowires, over devices known as Interworking Functions (IWF). Normal TDM equipment exists at both ends of the connection. Timing frequency is recovered exactly in the same manner as in conventional TDM, given that it is simply TDM traffic that is being transported over an Ethernet pseudowire. The quality of the recovered timing is determined by the IWF and the method(s) used.
- IEEE1588 Precision Time Protocol (PTP): PTP is a two-way time transfer protocol wherein a Grandmaster clock is synchronized to a high quality source, such as GPS, and then generates packets with precise timestamps that are sent downstream to slave devices. The slave devices use these timestamps as well as a delay request and response conversation to derive the clock that is supplied to the equipment requiring synchronization. Devices between the master and slave clocks may be ordinary switches and routers, or specialized equipment with *on-path support*, such as Boundary Clocks and Transparent Clocks, which are intended to mitigate the effects of timing impairment introduced by the network between the master and slave.
- Synchronous Ethernet (’SyncE’): Uses the bit clock of the Ethernet physical layer to provide frequency synchronization. ESMC frames are sent between the SyncE EEC devices to advertise clock quality and other *synchronization status messages* (SSM).
- These different methods may be used independently or in conjunction with one another. Hybrid networks that intentionally use more than one technology to leverage the strengths of each are increasingly being deployed, notably PTP with SyncE.

Technology Alternatives

The following technologies can add a clock distribution capability to Ethernet:

Network Timing Protocol (NTP) has evolved (NTPv3, RFC 1305 and SNTPv4, RFC 4330) and is used extensively in systems that require clock synchronization to an accuracy of 1-50 ms. Better accuracies require carefully controlled switches, clients, and servers. Recognition of NTP's fundamental limitations helped lead to the development of IEEE1588 Precision Time Protocol (PTP).

Global Positioning System (GPS) technology is used extensively in CDMA wireless base stations and many other applications to provide frequency and time synchronization. However, GPS receivers require setup of an antenna with adequate sky view. This can be impractical in many home, business, and central office (telecommunication) environments.

Hybrid T1/E1 and Ethernet systems use one or more legacy T1 or E1 links to provide clock synchronization (syntonization only) and use Ethernet to expand bandwidth more cost-effectively. This is not cost-effective for new installations.

IEEE1588, Synchronous Ethernet, and **Hybrid** systems are favored but face their own implementation challenges that are described later in this book.

Applications Requiring Synchronization

There are many new and evolving applications that need synchronization. These include:

- **Wireless backhaul**: "Wireless backhaul" refers to the path in the radio access network between the base station (Node B) and an upstream node, such as a base station controller (Radio Network Controller). Ethernet is replacing and augmenting legacy T1/E1 links along these paths.
  Wireless Frequency Division Duplex (FDD) systems generally require only frequency stability and lock (syntonization) of base stations. Time Division Duplex (TDD) systems, however, generally also require time-of-day (also known as "wall clock") alignment.
- **Femtocell**: Service providers can extend network coverage to the interior of homes and small businesses by using small cellular base stations and taking advantage of existing DSL, cable, or Ethernet access for the backhaul. Although standards bodies (such as 3GPP) are relaxing the frequency precision requirements for indoor base stations, there is still a need for a low-cost synchronization mechanism to replace GPS receivers and ovenized oscillators.
- **Carrier Ethernet**: Other carrier applications requiring synchronization include Circuit Emulation Services (**CES**) and Passive Optical Networks (**PON**).
- **Data centers**: Data center operators are being driven to deploy low-latency Ethernet switches and to log and timestamp packet data so that financial transactions can be accurately traced, and to offer services to derivatives traders whose profit relies on being able to set online trades milliseconds faster than their competitors.

- **Industrial Automation**: There are a multitude of needs for the synchronization of industrial equipment within segments such as power, transport, process control and manufacturing automation. Manufacturers and system integrators are increasingly standardizing on Ethernet for the advantages of cost and equipment availability.
- **Test and measurement systems**: LXI (LAN eXtensions for Instrumentation) Class A and B devices use IEEE1588 to provide time-stamped data logging and measurement triggering across a standard Ethernet LAN.
- **Military/aerospace/defense**: Specialized Ethernet switches that include IEEE1588 Transparent Clock capabilities are already replacing IRIG-B and GPS for clock synchronization in environments that require ruggedized network equipment.
- **Audio Video Broadcasting** (AVB): The IEEE is developing a set of standards in 802.1 to allow transport of time-sensitive data and the synchronization of multiple media streams for applications such as digital video, high-fidelity digital audio and gaming.

The table below lists the frequency and time transfer performance goals for a few of these applications.

Table 1. Syntonization and Synchronization Performance Goals for Example Applications

Example Application	Relevant Standard	Frequency Requirement	Time-of-day (Phase) Requirement
CDMA 2000	3GPP2 C.S0010-B, C.S0002-B	50 ppb	3 µs; 10 µs worst-case
UMTS TDD	TS 125.105	50 ppb	2.5 µs between base stations; 1.25 µs from a common source
UMTS FDD and GSM FDD	3GPP standards	50 ppb	Not applicable
TD-SCDMA	3GPP TR 25.836	50 ppb	3 µs
WiMax	IEEE 802.16	2 ppm	5 µs suggested for TDD
DVB-T/H SFN		Few ppb (depends on radio frequency)	1 µs
LTE Multimedia Broadcast over SFN	3GPP		3 µs

Note: The above requirements generally apply to the radio interface at radio base stations. A much tighter frequency or timing budget (e.g., 16 ppb, as per ITU-T G.812 Type II) may be required to be allocated to the network or to individual network devices.

Source: IEEE1588v2 telecom profile framework, IETF draft-ji-tictoc-1588-telecom-profile-framework-01.txt, Feb 2008.

Testing Ethernet Synchronization

Network operators and service providers must test their equipment and networks before deployment to ensure interoperability, applicability of the design for the intended application or purpose, and to maximize revenue and customer's quality of experience. Likewise, the equipment manufacturers must test their equipment before presenting it to their customers, the network operators, and service providers. Vendors of Ethernet hardware and silicon solutions (for example, PTP-enabled Ethernet PHYs and PTP protocol stacks) must also test their equipment to sell to the equipment manufacturers. Test laboratories also test solutions to establish the quality or applicability of this equipment before deployment. Given the tremendous growth of revenue that is expected in mobile network bandwidth and deployment, comprehensive pre-commissioning testing of the equipment is imperative.

The ITU-T, ETSI, and IEEE, among others, provide standards that specify limits and methods of testing for Carrier Ethernet technology. New standards and amendments are being added continuously as development of this technology progresses.

When evaluating the synchronization of a network or device, in addition to validating the basic functionality, it is important to verify synchronization performance as well as scalability.

Key functional, performance, and scalability test cases include:

- Synchronization performance: Frequency and Time of Day/Phase
    - Test to ITU-T Standards: G.826x and G.827x
- IEEE1588/PTP Time Error
- PTP scalability (testing the number of Slave Clocks that can be supported under various message rates)
- Best Master Clock (BMC) selection and failover
- Transparent Clock Correction Field Accuracy measurement
- PTP Packet Prioritization (layer-2 and layer-3 QoS)
- Multiple clock-domain scalability, and inter-domain interactions
- Control-plane loads, protocol interactions, and network instabilities
- Service disruption (failover testing)
- Negative (abnormal) testing and additional stresses:
    - Message timing (response to 'slow message turnaround' such as sending FollowUp after a configured time interval after sending Sync)
    - Stability while receiving abnormal PDUs
    - Message disabling

To completely test the network synchronization, two types of test equipment must be used together:

- Ixia Anue 3500 provides comprehensive packet-layer and physical-layer timing impairment, analysis, and measurement for synchronization networks and devices.
- IxNetwork provides protocol emulation for IEEE1588v2 and ESMC to validate the protocol functionality, performance, and scalability of synchronization networks and devices.

Terminology, Measurement Methods, and Metrics

Terminology

Before discussing details of testing synchronization in packet networks, it is important to understand what we mean by ’timing transfer.’

Syntonization is the process of setting the **frequency** of one oscillator equal to that of another. Two clocks are syntonized if the duration of the second is the same on both, which means that the time as measured by each advances at the same rate. They may or may not share the same epoch (origin of timescale), that is, the clocks may be out-of-phase and have no need for time-alignment.

Synchronization is the coordination in **time** between a transmitter and a receiver. Two clocks are synchronized to a specified uncertainty if they have the same epoch (origin of timescale) and their measurements of the time of a single event at an arbitrary time differ by no more than that uncertainty.

Frequency is the number of cycles per unit time; the reciprocal of the time taken to complete one cycle. Frequency is expressed in Hz.

Phase is the relationship between two time-varying signals. In the case of network synchronization, phase is normally expressed in terms of time, such as nanoseconds (ns).

Time of Day is a count of the number of seconds from a prescribed point in time, represented as normal ’wall clock’ time and ’calendar’ date. Local time is adjusted from UTC according to your time zone.

> **UTC:** Coordinated Universal Time, previously referred to as Greenwich Mean Time (GMT)
>
> **GPS:** Global Positioning System time; atomic time scale implemented by atomic clocks in GPS ground control stations and satellites, beginning at 0h on Jan 6, 1980. No leap seconds; 16 seconds ahead of UTC.
>
> **TAI:** Temps Atomique International; based on a continuous counting of seconds since Jan 1, 1970; 35 seconds ahead of UTC because of leap seconds; always ahead of GPS by 19 seconds.
>
> Source: leapsecond.com

Measurement Methods and Metrics

Packet Delay Variation

Packet Delay Variation (PDV) is the variability of delay packets experience because of queuing and traffic conditions in the network. PDV may also be known as ’packet jitter.’ PDV is a

property of a network, and not specifically a property of a device. However, the devices on the network are the ultimate cause of the PDV, because of differences in queuing and delay due to integration of PTP traffic with background traffic, or because of other design considerations that lead to differences in delay or timing of PTP packets as they are forwarded through the device.

PDV is normally measured with Packet TIE metrics, and derivatives of the packet TIE may be viewed as a histogram showing delay distribution, or in terms of Floor Packet Population metrics, which identify the number of packets in a given interval of time that experience a minimum of delay.

PDV can lead directly to physical-layer wander in synchronization networks, because PTP devices recover their frequency from PTP sync and follow-up packets that are subject to PDV. This recovered frequency, which may have an error, is used to synchronize other equipment in the network. For this reason, the PDV must be tested to ensure performance of packet-based synchronization networks.

Wander

Wander refers to the physical-layer deviation of a clock signal compared with the reference or source clock. Wander is differentiated from jitter, in that wander is the term applying to periodic deviations at a frequency below 10 Hz, and jitter refers to deviations above 10 Hz. Wander can indicate a frequency offset, if it is linear, or it may indicate a periodic effect, if it is time-varying, and is therefore viewed in terms of frequency.

Wander is a property of a physical clock. While packet-layer impairments such as PDV can lead to wander, wander occurs at the physical layer, and not at the packet layer. Clocks that are derived or recovered from Ethernet packet networks may have wander that result from the PDV in the network.

Wander is typically measured with Time Interval Error (TIE). Many statistical metrics can be derived from TIE data, and the most commonly-used are MTIE and TDEV. Wander must be evaluated by using TIE, MTIE, and TDEV metrics. A number of ITU-T standards provide limits for MTIE and TDEV, known as masks, which are used to test wander on network synchronization clocks.

MTIE and TDEV

Wander is typically evaluated by using two metrics: MTIE and TDEV. MTIE and TDEV are derived from the raw TIE data. Normally, the amplitude of MTIE or TDEV calculation is represented in units of time (ns), graphically plotted on the Y axis, against an observation interval ’tau,’ which is plotted on the X axis.

To calculate MTIE and TDEV, TIE data is analyzed in progressively larger windows or intervals of time, which are plotted on the X axis. ’Tau’ is the width (in time) of this window from which the value of MTIE or TDEV is calculated. While tau is related to time, it is not the same as time.

MTIE: Maximum Time Interval Error

MTIE is a measure of the maximum difference of any two data points in the TIE data within the given value of tau. MTIE can be a useful indicator of buffer size or cumulative frequency offsets.

TDEV: Time Deviation

TDEV represents the spectral content of the TIE (the frequencies of wander present on the clock, and the magnitude of these frequencies). TDEV is a useful indicator of periodic effects present in TIE data.

Time of Day/Phase

Time of Day – the real time

PTP devices use nanosecond-accurate timestamps for frequency recovery. These time stamps indicate the precise real time in seconds and nanoseconds from a prescribed point in time (for PTP and TAI time, this is Jan 1, 1970). Since they are real-time, the actual current time of the day can be calculated directly from each PTP packet.

Phase – using '1PPS'

1PPS is an electrical signal with one electrical pulse per second that precisely identifies the beginning of a second. This allows the time of day of a clock to be set precisely to the correct time. Since PTP delivers time stamps with nanosecond accuracy, whole seconds can be derived easily.

Delays in the network may result in an error in time of day recovered by the PTP protocol, and this error is reflected in the 1PPS signal produced by the device. PTP slave devices, including boundary clocks and ordinary clocks, must compensate for this error, or their time base will be incorrect.

Time of Day – GPS-derived

Accurate Time of Day (ToD) is delivered by GPS satellites, and GPS time is commonly used not only by PTP grand master clocks, but also as an alternative to PTP for mobile network installations. GPS receivers communicate this time of day by using serial interface and 1PPS pulse. Many GPS receivers are also equipped with a high-precision oscillator such as a rubidium clock, which can be used to deliver a frequency signal such as 10MHz or 2.048MHz in addition to the ToD and 1PPS signals.

The ToD information is communicated over a protocol such as NMEA or CMCC over RS232/RS422 connections. This signal communicates what the actual time is at the next pulse. The following 1PPS pulse provides precise alignment.

Testing Ethernet Synchronization Protocols

Ethernet Synchronization protocols are basic foundation of Timing Synchronization over packet network. Proper protocol implementation ensures basic interoperability of delivering timing information across the packet network for end-to-end synchronization. The protocol scale and performance also ensures that the protocols are functional at high scale with acceptable performance in real network conditions.

Ethernet Synchronization Message Channel (ESMC)

Synchronous Ethernet (SyncE) uses ESMC protocol (described) for clock selection, distribution, management, traceability, and failover. It uses Synchronization Status Message (SSM), which carry a Quality Level (QL) identifier to communicate current reference-clock quality between nodes. A SyncE device processes SSM messages from various ingress ports and selects a port with the highest clock quality. The clock derived from the selected port is used as the reference clock. The ESMC and SSM message format is defined in ITU-T G.8264.

The implementation and configuration of this protocol must be accurate, robust to malicious and badly formed packets, scalable to handle large networks, and of high performance to ensure rapid clock failover following an upstream clock or switch failure.

IEEE1588v2 (Precision Time Protocol)

The IEEE1588v2 defines a Master-Slave hierarchy to deliver clock information in dedicated timing packets across packet network. The synchronization packets do not depend on the network traffic and are always exchanged between Master and Slaves. The IEEE1588v2 not only provides frequency synchronization, but also provides Time of Day (ToD) and phase synchronization.

There are several PTP modes of operation:

- PTP can be transported over Ethernet/VLAN, IPv4, and IPv6.
- PTP can operate in Unicast, Multicast, and Mixed Unicast/Multicast communication modes.
- PTP can operate in 1-step and 2-step modes.
- The Delay Mechanism can be Request-Response and Peer Delay.

There are also several types of PTP devices:

- Master
- Slave
- Boundary
- Transparent

All the PTP operation modes and device types need to be qualified for proper function, scale, and performance.

There are many test challenges that must be addressed during the development and deployment of PTP devices. A PTP device must implement proper PTP protocol behaviors for various operation modes and ensure that they function at scale condition. It is also required to be tested in conjunction with other protocols and network traffic. The most complex of these challenges are covered within the test cases described in this section.

Test Case: PTP Scalability by Using IxNetwork

Overview

In most PTP systems, there are multiple Slave Clocks. For example, in a wireless network, each cell site might include a Slave Clock. As the number of Slave Clocks in the system increases, the load on the Grandmaster Clock (or upstream Master Clock) increases, and at some point, it may be necessary to introduce Boundary Clocks to enable the system to scale further.

Therefore, as a part of the system design and before any deployment or system upgrade, **it is crucial to benchmark the scalability** of each type of Master Clock, Boundary Clock, and (for similar reasons) Transparent Clock.

Using Ixia applications IxN2X and IxNetwork, you can easily emulate large numbers of Slave Clocks and measure the number of Slave Clocks that the DUT can handle under realistic or extreme conditions.

If your system uses multiple clock domains, you can also use IxN2X or IxNetwork to emulate Master Clocks on multiple clock domains to verify the ability of Slave Clocks, Boundary Clocks, and Transparent Clocks to scale across multiple clock domains.

The ultimate scalability of your DUT will depend on many factors, such as the Sync message rate, the Delay-Request message rate, and whether Unicast or Multicast mode is used. Pay particular attention to the test variables listed at the end of this test case, and create a test plan that verifies your DUT’s scalability under both realistic (expected) conditions and extreme or worst-case conditions.

Objective

This test measures the number of Slave Clocks that can be supported by a Master Clock, Boundary Clock, or Transparent Clock DUT.

This example describes the setup and steps needed to test a Master Clock DUT. If your DUT is a Transparent or Boundary Clock, you may also set up and configure one or more emulated Master Clocks.

Setup

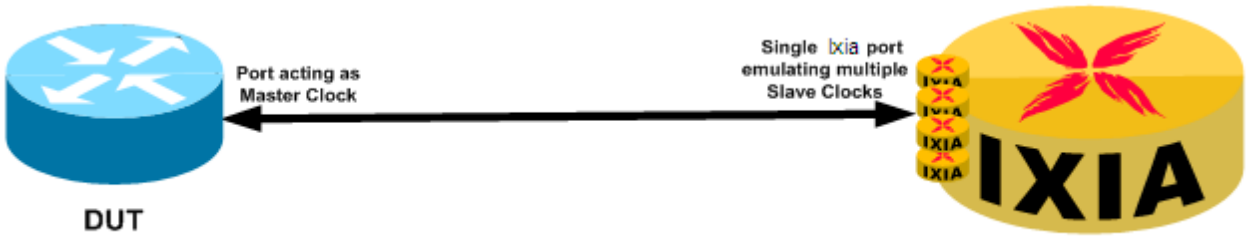


Figure 1. PTP Scalability test setup

Configure the DUT and Ixia as follows:

- Configure the DUT with one port that will act as the Master Clock. We will call this port the DUT's Master port.
- Configure the Ixia with one test port, on which multiple Slave Clocks will be emulated. We will call this port the Ixia Slave port.
- Connect the DUT Master port to the Ixia Slave port with an Ethernet cable.

Step-by-Step Instructions

The following step-by-step instructions use IxNetwork and a DUT to perform the PTP Scalability test:

1. After reserving the IxNetwork test port, start the **PTP Wizard** by double-clicking **PTP.**

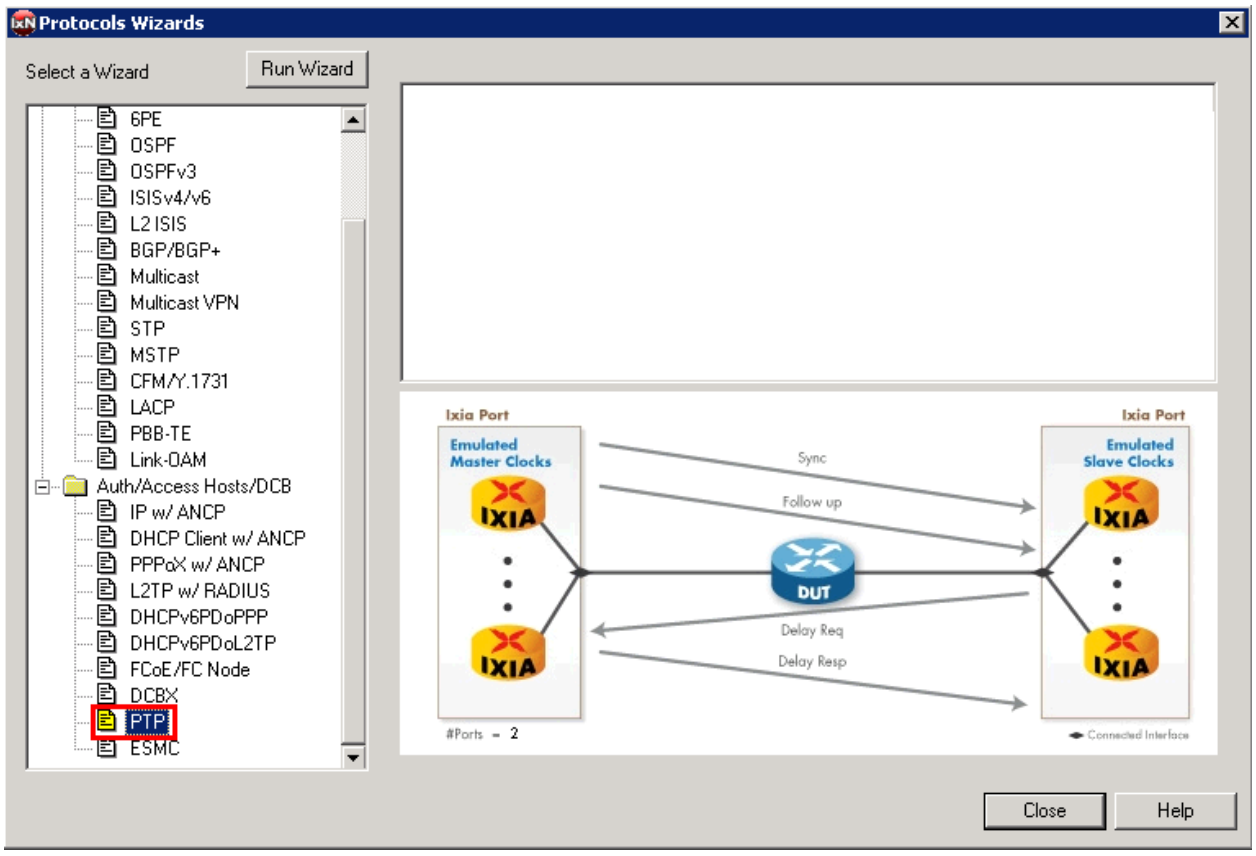


Figure 2. PTP Wizard - Initial Screen

2. On the first page of the PTP wizard, configure key PTP settings and the role of the IxNetwork tests port(s). The 'PTP Scenario' defaults shown are common with many PTP devices, however, ensure that they match the DUT, or the Slaves may not be able to communicate with the Master.

   a. Change the **Role** of the port to **Slave**.

   b. Change the **# Ranges per Port Group** to **2**. This will create two unique ranges of PTP Slaves on the port. The number of Slaves per port depends on the **Addresses per Range** setting on the next screen.

   c. Optionally, use the lists on the other options to change key PTP settings.

Note: The wizard can only configure one *Role* at a time, so if Masters and Slaves are needed in the test, at least two runs of the wizard are required.

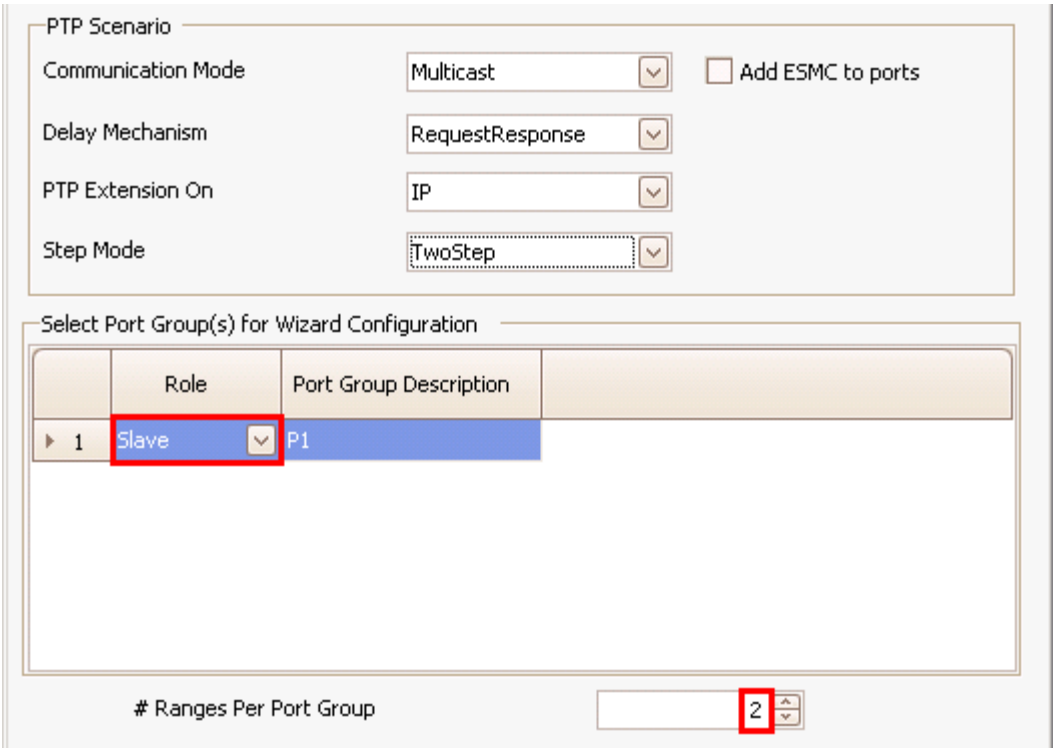


Figure 3. **PTP Wizard - Page 1**

3. The second page of the PTP wizard (mainly) configures the addressing (of the slaves), and the quantity of slaves. Note that IPv6 is also supported.

   a. Change the **Addresses per range** to 25.

      This will configure a total of 50 slaves across the two ranges. As this test determines the maximum number of Slaves supported on a single Master, we will start with 50 and go up from there. One way to do this is to run the wizard again and add more ranges and addresses per range. Another way (shown in a later step) adds more ranges in the post-wizard configuration.

b. Change the **Mask** to 16 to accommodate enough address space to scale the Slaves.

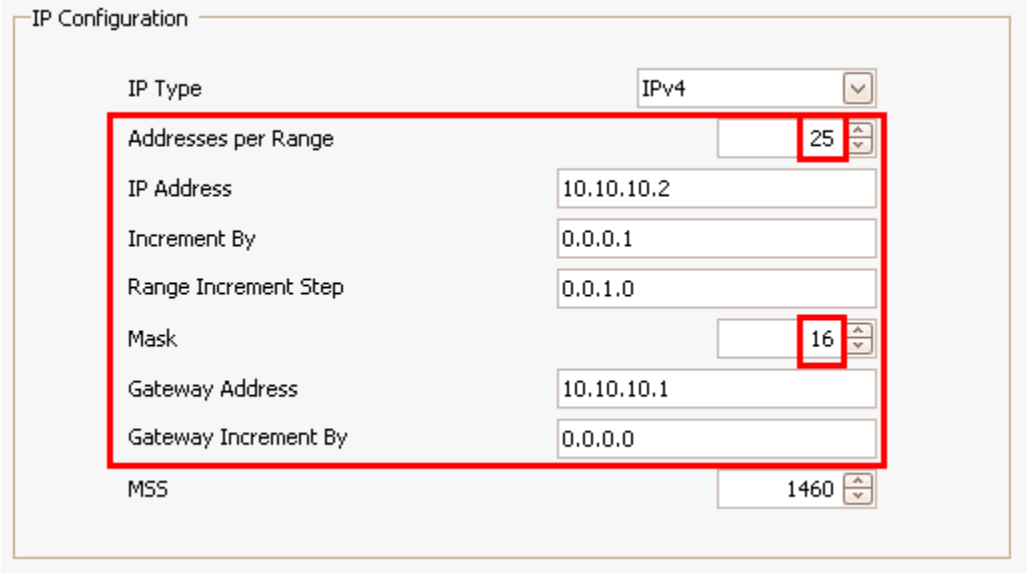


Figure 4. **PTP Wizard - Page 2**

4. The third page of the PTP wizard configures the Clock Identity of the slaves. If this wizard had been run with Masters selected on the first page of the wizard, this page would also serve to configure **Negative Testing** and **Best Master Clock Settings** of the Master.
   a. (Optional) Select the **Use Clock Identity** check box to configure the Initial, Increment, and Range Increment of the Slaves. Typically, Slaves use their MAC address followed by unique 2-bytes of Hex, but this can be overwritten with this field.

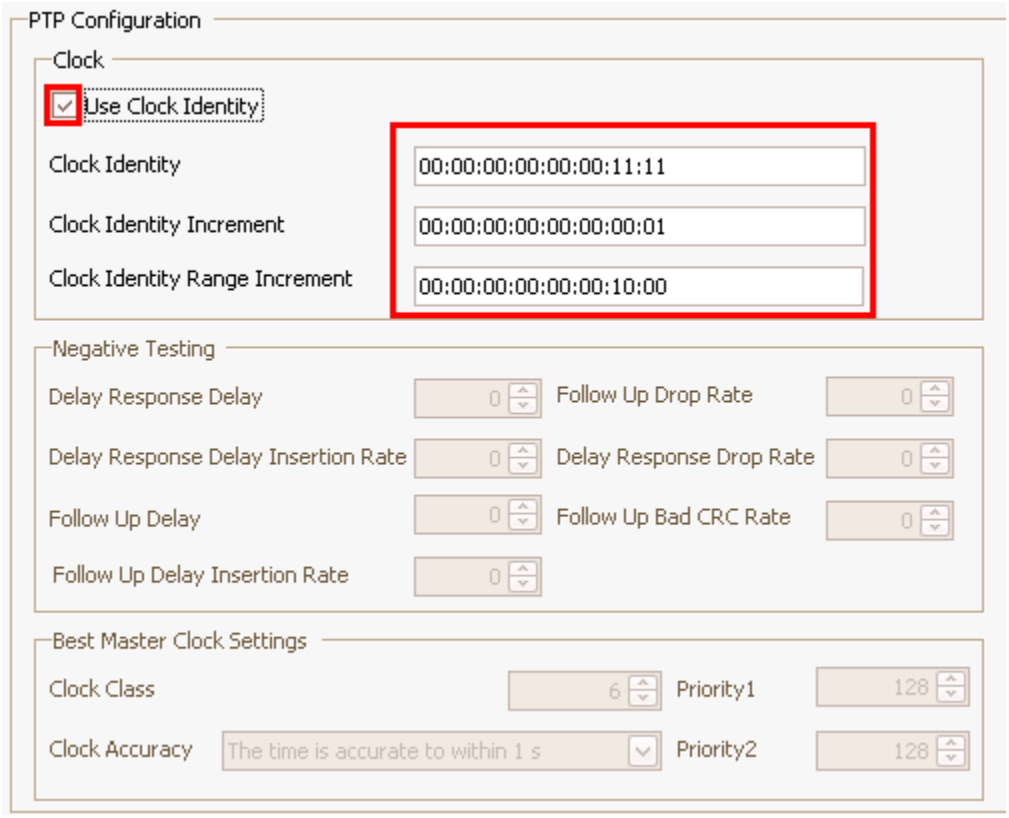


Figure 5. **PTP Wizard - Page 3**

5. The fourth page of the PTP wizard configures the MAC addresses of the Slaves.
   a. (Optional) Configure the MAC address of the First, Increment, and Range Increment of the Slaves.

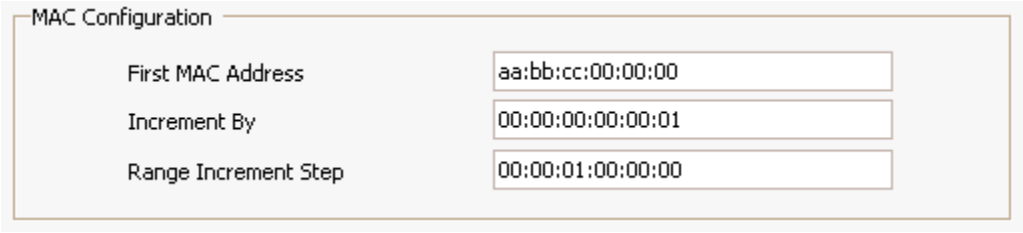


Figure 6. **PTP Wizard - Page 4**

6. The fifth page of the PTP wizard adds VLANs.

   a. (Optional) Select the **Enable Outer** and Enable **Inner** check boxes.

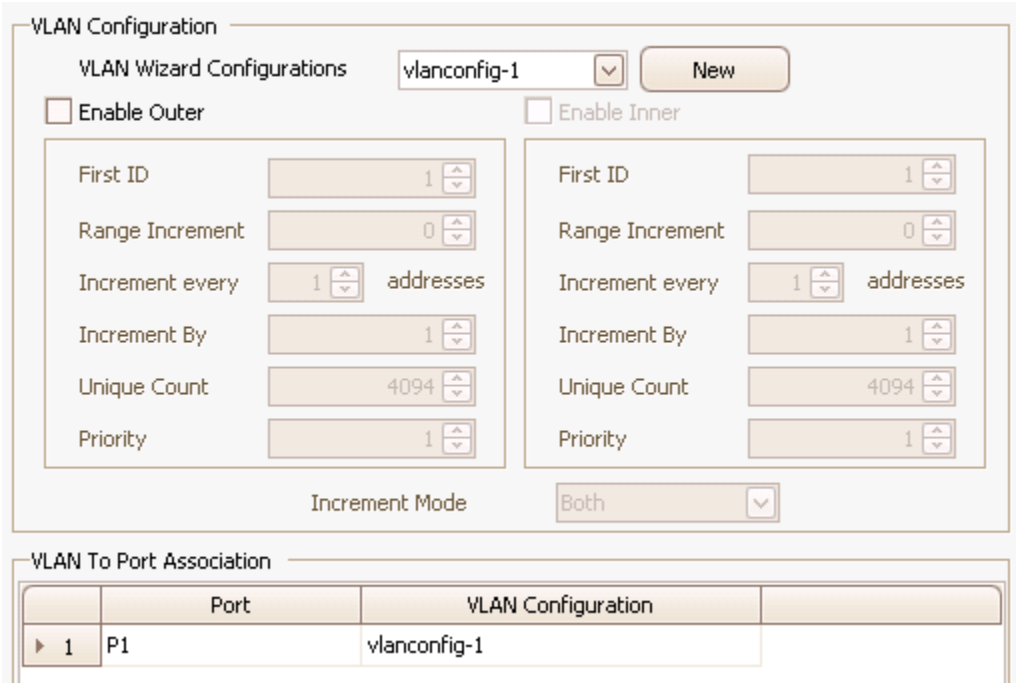


Figure 7. **PTP Wizard - Page 5**

7. On the sixth, and last page of the PTP wizard, configure a **Name** for the parameters just used in this wizard, and select how to apply those parameters.

   a. Configure a name, such as *BlackBook PTP Scalability Test Case*.
   b. Click **Generate and Overwrite** and select the **Identical protocol stacks** option. This will overwrite any PTP stacks that are already configured on Port *P1.*

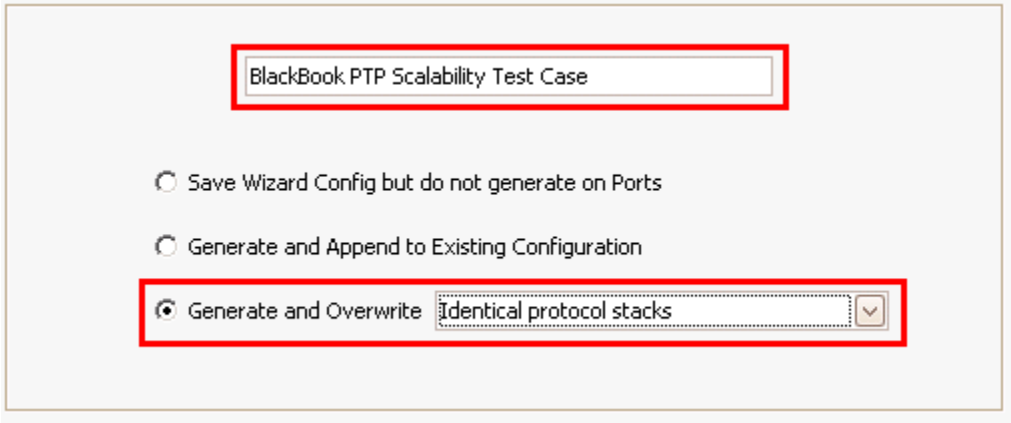


Figure 8. **PTP Wizard - Page 6**

8. After clicking **Finish**, close the wizard and view the wizard configuration in the main IxNetwork GUI.
   a. Go to **Auth/Access Hosts/DCB -> Static IP/w/Auth -> Static IP -> PTP** to see the two ranges of 25 slaves that were created.
   b. (Optionally) Scroll to the right to view or change the settings of each Slave range.
   c. (Optionally) Click the **IP** or **MAC** tabs at the bottom to see the lower layer configuration of the slaves.

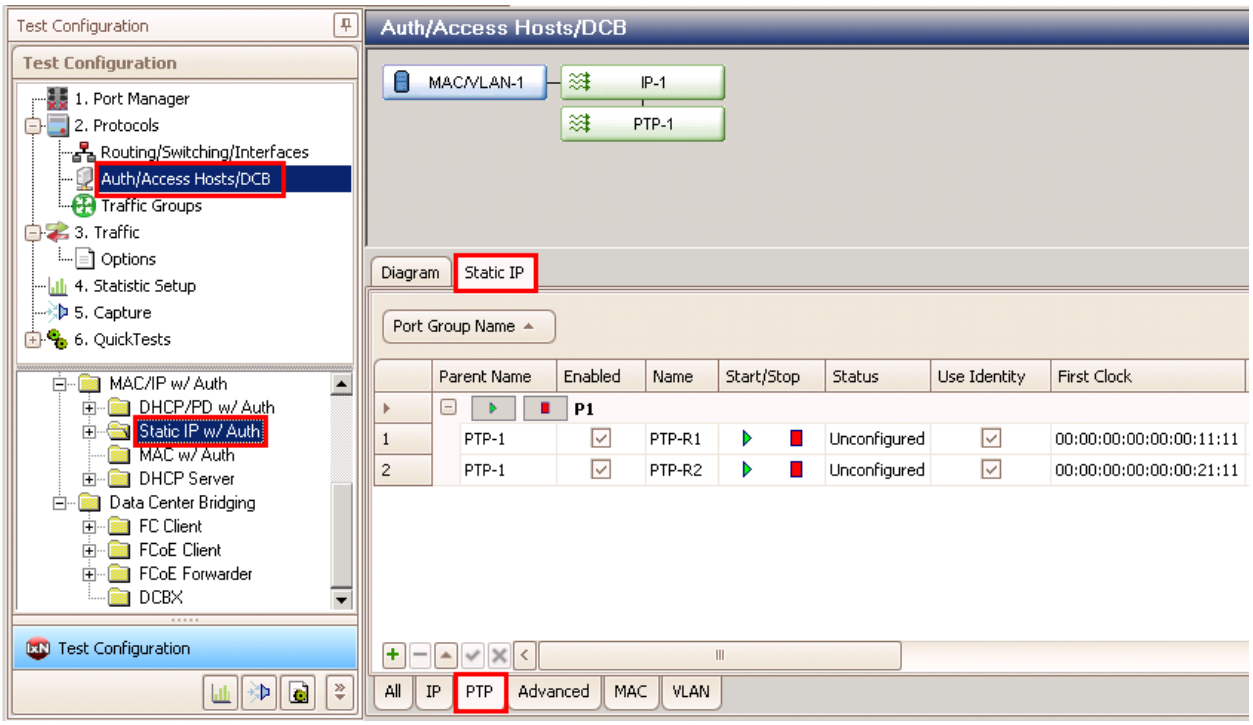


Figure 9. **Post Wizard Configuration screen**

9. Start the Slaves.
   a. Start the Slaves by clicking the green arrow button(s). The top green button will start all the ranges, and the lower green buttons will start one range at a time. The **Status** column should change to *Negotiated when* the PTP protocol is running on the Ixia port(s).

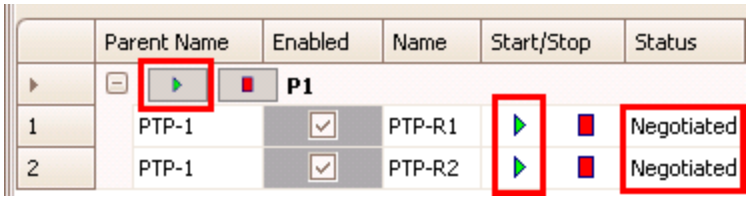


Figure 10. **Start PTP Protocol**

10. View the Statistics of the Slaves. Aggregate and per-Slave statistics are available.

a. On the lower left of the main IxNetwork window, click **Statistics** 

.

b. Open the **PTP** and **PTP Per Session** statistics.

i. To open the **PTP Per Session** statistics, right-click the **PTP row** and select **Drill Down per Session.**

ii. You can also right-click **Per Range** to see aggregate results for each range of 25 slaves.

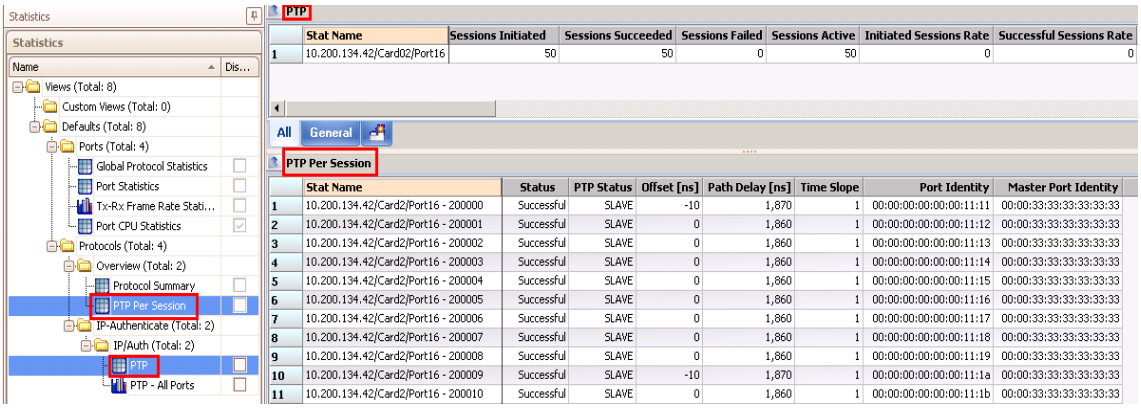


Figure 11. PTP Per Session Statistics

11. Additional **per range/session** statistics can be added to the statistics view.

a. Hover the mouse over the **PTP Per Session** as shown in the following figure, click the **Filter/Sort** list, and then add the required statistics.

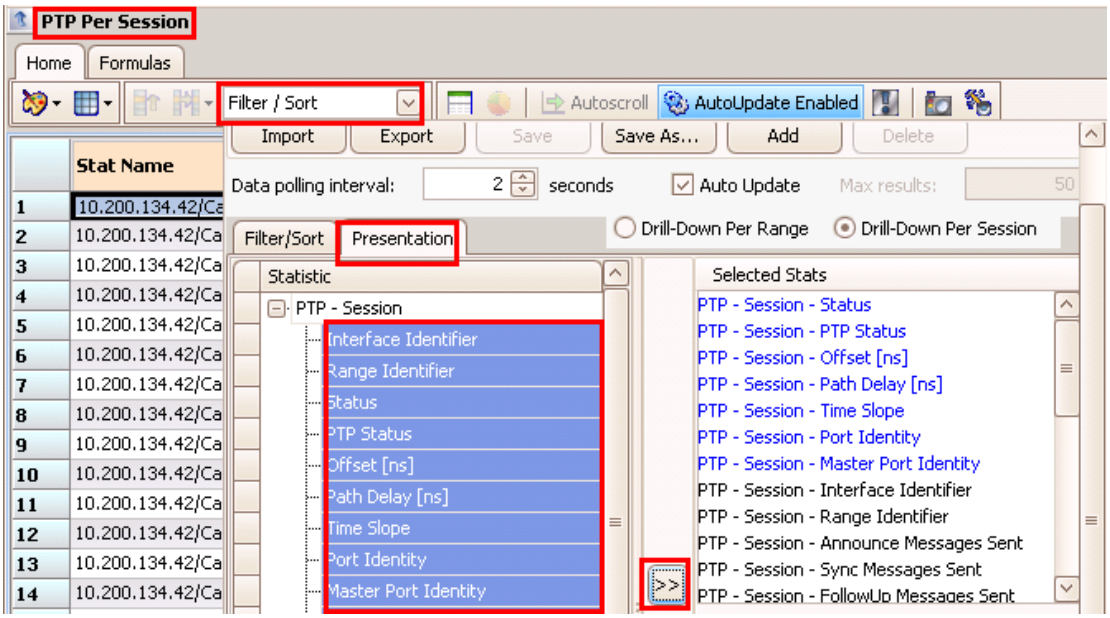


Figure 12. Adding more PTP statistics

12. Ensure that the Master is able to maintain the (50) slaves over a period of time.

    a. Monitor the **PTP Status** column of the statistics to see if they fall out of the *Slave* state.

    b. Monitor the **Sessions Active** field to see if it falls below *50*. To monitor this statistic automatically, define an **Alert** (right-click *50*) to give an alert if the value changes from *50* to any other number.

    c. Monitor the *Delay Request Messages Sent,* and *Delay Response Messages Received*. These values should remain the same; else, there may have been packet loss.

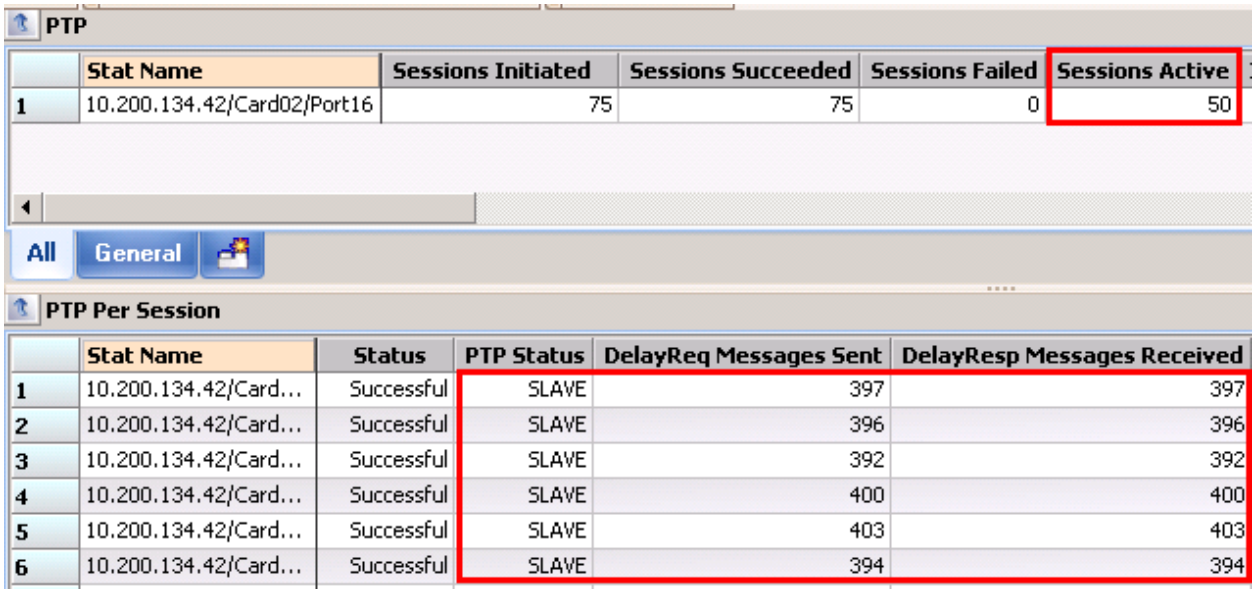


Figure 13. **Ensuring PTP Slave statistics**

13. Increase/Decrease the number of Slaves.

    a. Go back to step 8 and increase the Slaves by clicking the plus sign to add additional ranges of slaves. Ensure that the **PTP, MAC,** and **IP** settings are unique and correct and do not overlap each other.

        i. Another way to increase the slaves is by running the same wizard again, double-clicking the name of the wizard (**BlackBook PTP Scalability Test Case)**, and increasing the **# of ranges** and **Slaves per range** respectively.

    b. For each increase or decrease in slaves, repeat step 12 to ensure that the Slaves remain up over a period of time.

14. Repeat the test using a **binary search** to find the maximum number of slaves that can be supported by the DUT.

Table 2. Binary Search Example – Find the Maximum Number of Slaves that the DUT can Support

Number of Emulated Slaves	Test Run Result	DUT CPU Load
50	Pass	10 %
500	Fail	99 %
300	Pass	90 %
400	Fail	98 %
350	**Pass**	97 %
375	Fail	98 %

15. Repeat the entire test at a few different message rates, as shown in the following example table, to characterize the DUT under a range of conditions.

Table 3. Slave Scalability Results Example – Characterize Scalability Under a Range of Conditions

Sync Rate (messages per second)	Delay-Request Rate (messages per second)	Max # of Slaves
1	1	350
8	8	
32	1	

16. For additional troubleshooting and validation of PTP elements, use the capture/analyzer tool.

    It can automatically filter out unrelated protocol messages, providing a clear trace of the conversations between PTP endpoints, in real time. The tool captures both incoming and outgoing PTP messages, with on-the-fly filters to quickly find a specific packet.

The Expanded Decode of the PTP packet (DelayRequest message) is shown in the following figure.

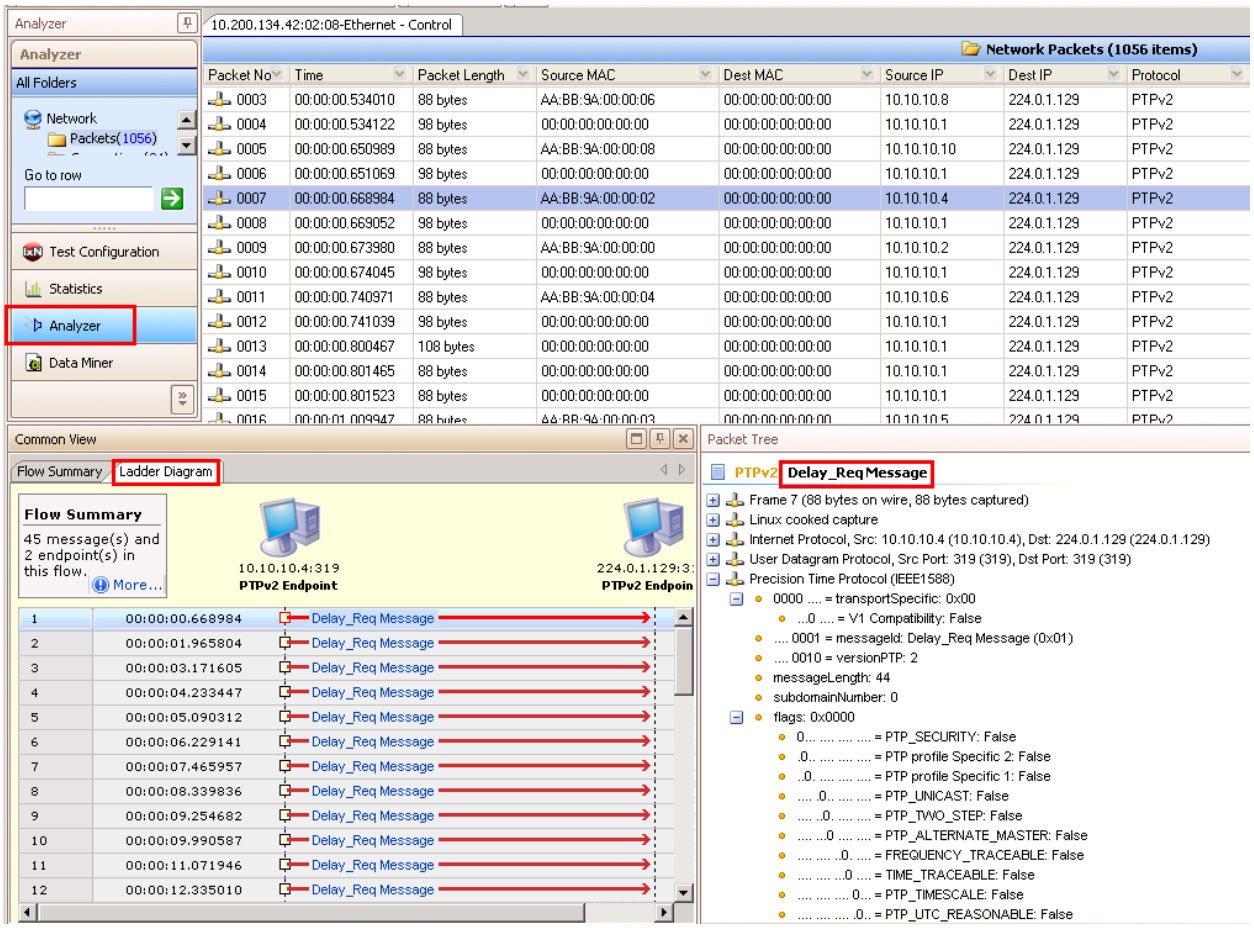


Figure 14. **IxNetwork Analyzer – PTP packets**

Test Variables

Repeat the test with the following suggested variations:

- Test with **multiple clock domains**. This will gauge the DUT's scalability while handling multiple domains at the same time.
- Test with two or more Ixia ports, and verify the PTP Slave scalability of the DUT across multiple ports.
- Test with the system in both PTP **multicast** mode and in PTP **unicast** mode.
- Test with the system in both **one-step mode** (which reduces the number of messages) and in **two-step mode**.
- Test with DUT in Master Clock, Boundary Clock, or Transparent Clock modes.
- Add a second Ixia port and send real-world user traffic (Data Plane) between the two Ixia ports. This would test the DUTs ability to maintain maximum PTP scale while forwarding user traffic.

Results Analysis

The results showed how the maximum PTP scalability of the DUT acting as a Master Clock, and how many Slaves it could successfully maintain in a real-world environment.

Conclusions

Confidence in the scalability of each system component is vital to the operation of any IEEE1588 system.

Test Case: PTP Scalability by Using IxN2X

Overview

In most PTP systems, there are multiple Slave Clocks; for example, in a wireless network, each cell site might include a Slave Clock. As the number of Slave Clocks in the system increases, the load on the Grandmaster Clock (or upstream Master Clock) increases, and at some point it may be necessary to introduce Boundary Clocks to enable the system to scale further.

Therefore, as a part of the system design and prior to any deployment or system upgrade, **it is crucial to benchmark the scalability** of each type of Master Clock, Boundary Clock, and (for similar reasons) Transparent Clock.

Using Ixia applications IxN2X and IxNetwork, you can easily emulate large numbers of Slave Clocks and measure the number of Slave Clocks that the DUT can handle under realistic or extreme conditions.

If your system uses multiple clock domains, you can also use IxN2X or IxNetwork to emulate Master Clocks on multiple clock domains to verify the ability of Slave Clocks, Boundary Clocks and Transparent Clocks to scale across multiple clock domains.

The ultimate scalability of your DUT will depend on many factors, such as the Sync message rate, the Delay-Request message rate, and whether Unicast or Multicast mode is used. Pay particular attention to the test variables listed at the end of this test case, and create a test plan that verifies your DUT's scalability under both realistic (expected) conditions and extreme or worst-case conditions.

Objective

This test measures the number of Slave Clocks that can be supported by a Master Clock, Boundary Clock, or Transparent Clock DUT.

This example describes the setup and steps needed to test a Master Clock DUT. If your DUT is a Transparent or Boundary Clock, you may also set up and configure one or more emulated Master Clocks.

Setup

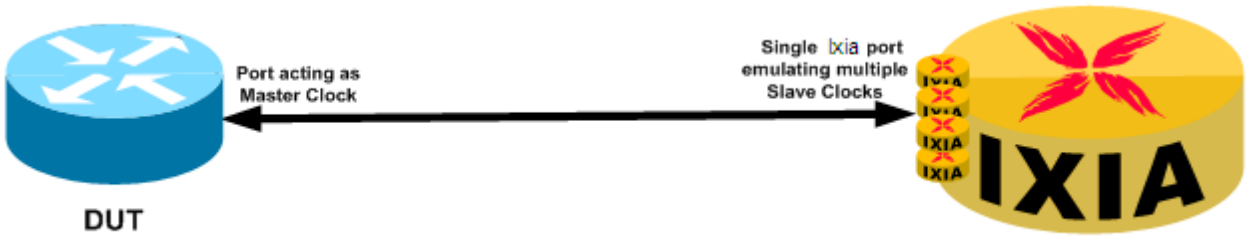


Figure 15. PTP Scalability test setup

Configure the DUT and Ixia as follows:

- Configure the DUT with one port that will act as the Master Clock. We will call this port the DUT's Master port.
- Configure the Ixia with one test port, on which multiple Slave Clocks will be emulated. We will call this port the Ixia Slave port.
- Connect the DUT Master port to the Ixia Slave port with an Ethernet cable.

Step-by-Step Instructions

The following Step-by-step instructions use the IxN2X and a DUT to perform the PTP Scalability test.

1. Within the **Tools** Menu, open the **Dashboard**. On the Dashboard window, click **On** to enable CPU and memory usage monitoring. Throughout the test, while the Slave Clock load is increased, this will allow you to check whether the IxN2X is the limiting factor. If necessary, take steps to lower the IxN2X CPU usage. For example, you may spread the applied load over multiple ports, which will require additional IxN2X test ports and either additional DUT ports or an Ethernet switch to aggregate and concentrate the load onto one DUT port.

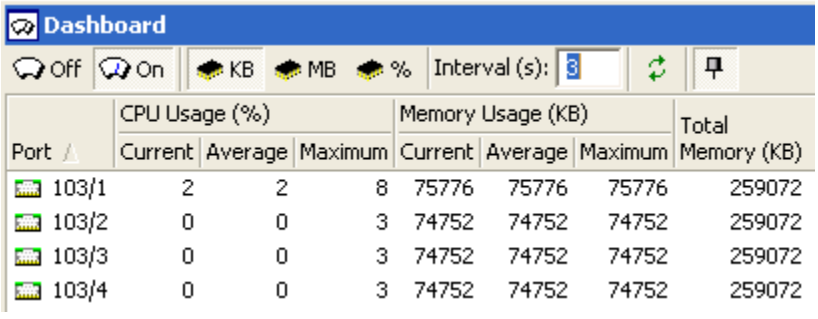


Figure 16. Use the IxN2X Dashboard throughout the test to monitor CPU usage

2. Configure the link layer and IP addresses of the IxN2X Slave port and of the DUT (Master Clock) port in a similar manner to test case **PTP 01 – Correction Factor Error**.

3. Create a Slave Clock pool with an initial 50 emulated Slave Clocks on the IxN2X with default parameters.

   a. In the main Setup Emulation window, select the port to be used as the Slave port, click **New**, and open the **PTP** emulation type. Select the **PTP Slave over UDP/IPv4** emulation type, check **Edit Properties after emulations added**, and press **OK**. The **Slave over UDP/IPv4 Properties** dialog will open.

   b. In the **Slave over UDP/IPv4 Properties** dialog, in the **PTP Slave Clock** tab, uncheck **Apply random distribution**. This will help ensure that the test is deterministic and repeatable, and will help prevent the overlap of Delay-Request and Delay-Response messages.

   c. In the **Slave over UDP/IPv4 Properties** dialog, in the **General** tab, change the **Count** to *50*. You will need to change the **Count** value many times during the test. This value can also be changed within the **Count** column of the **Setup-Emulation** main window.

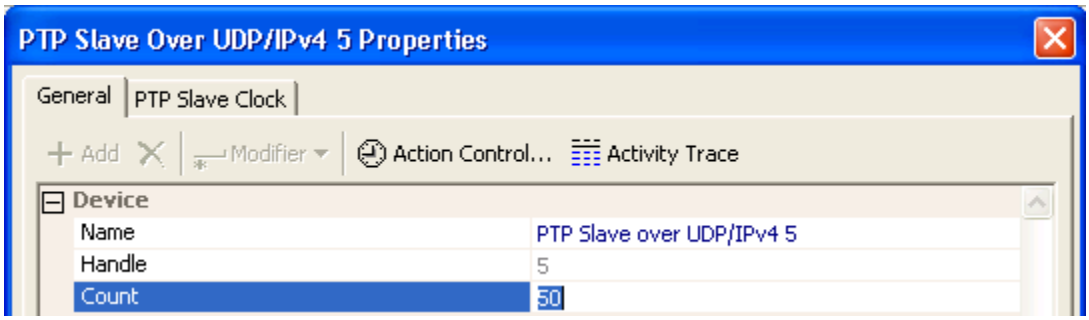


Figure 17. **Create an initial pool of 50 emulated Slave Clocks**

d. In the **Setup-Emulation** main window, right-click the Slave Clock emulations and, in the drop-down menu, select **Action Control…** custom command. Set the rate of Slave Clock emulations startup to 5 Slaves per 100 milliseconds, as follows:

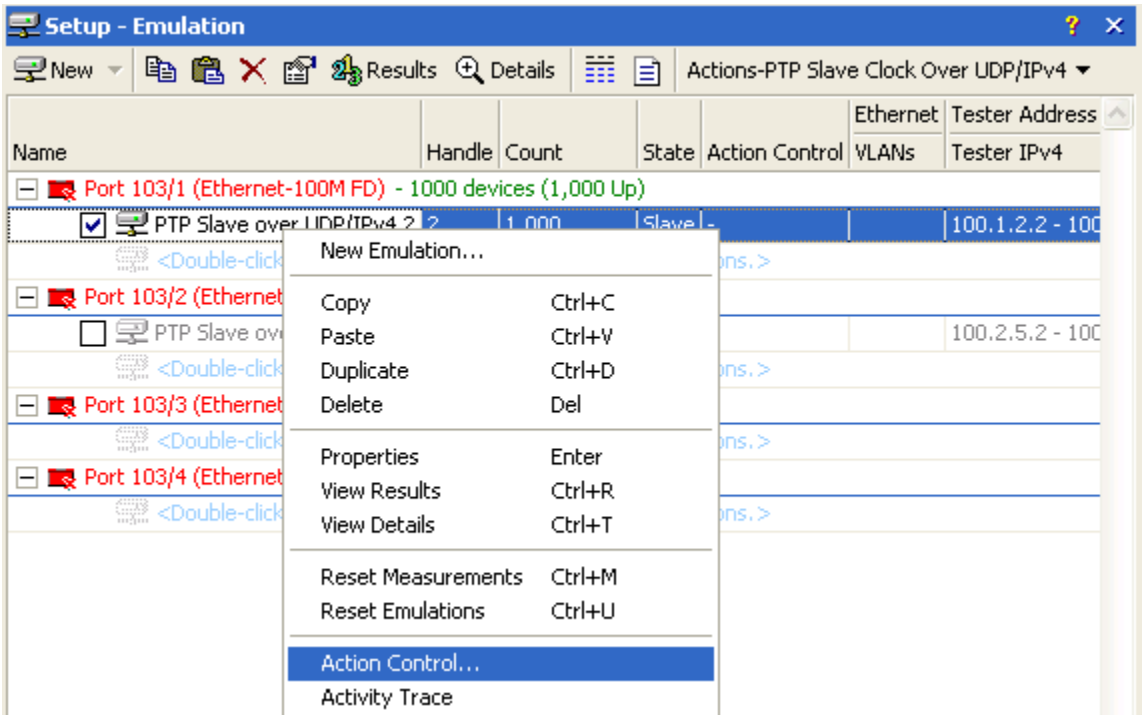


Figure 18. **Select Action Control by Right-clicking the Slave Emulations**

i. Under **Scheduling** Policy, set **Action** to **Enable Emulation** and set **In state** to **Disabled**.

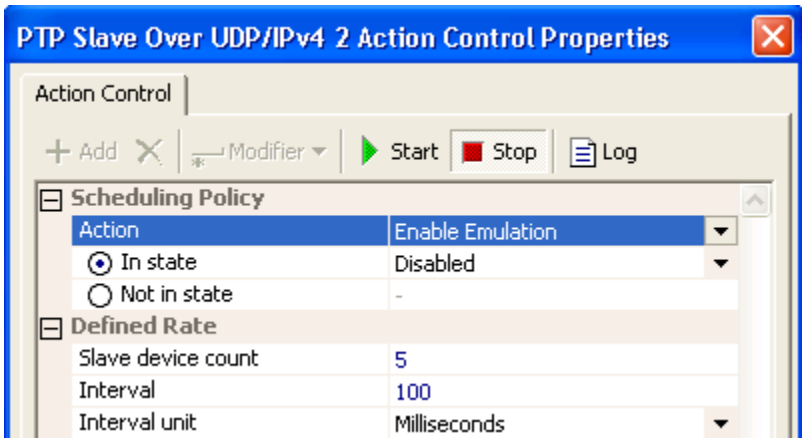


Figure 19. **Set the Action Control Parameters to Control the Startup Rate of the Emulations**

ii. Under **Defined Rate**, set **Slave device count** to *5,* set **Interval** to *100,* and set **Interval Unit** to **Milliseconds**.

iii. Hit the **Start** button.

e. Wait for all emulated Slave Clocks to reach the **Slave** state.

f. Right-click the slave emulations in the **Setup-**Emulation window and, in the drop-down menu, select **View Results**. The **Slave Results** dialog will open. Press the **Reset Measurements** button and, in the **Measurements** tab, monitor the **Delay response messages** and the **Delay request messages**.

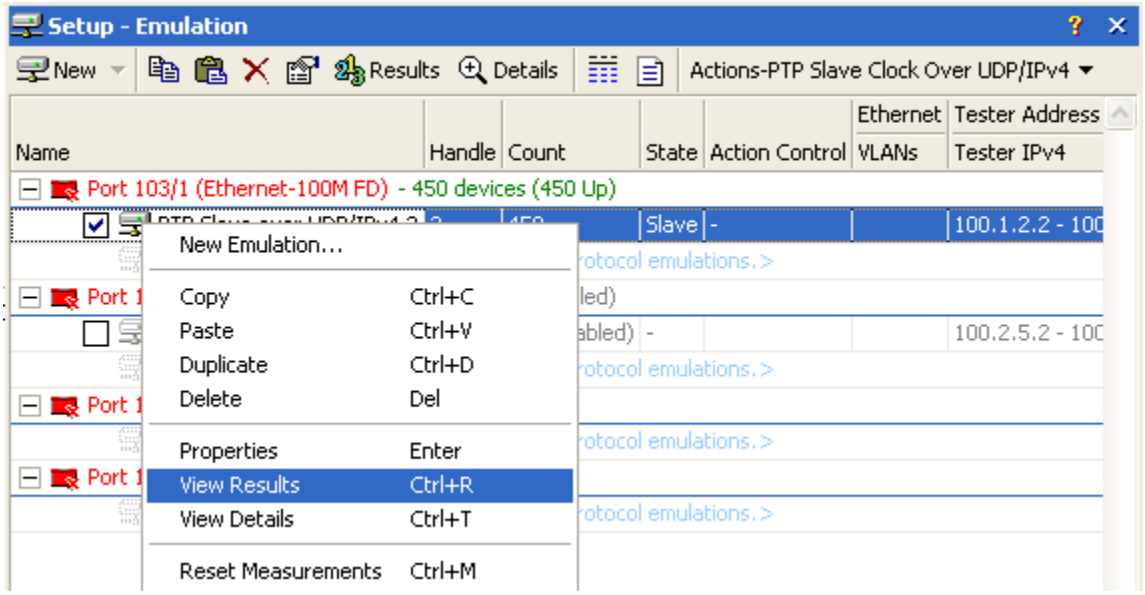


Figure 20. **Right-click the Slave Emulations and Select View Results to Open the Slave Results Dialog**

4. Determine the maximum number of slaves that can be supported by the DUT.

   a. A test run is considered to have passed if:

      i. All emulated Slave Clocks remain steadily in the **Slave** state.

      ii. Over a period of time, the number of **Delay response messages** sent by the emulated Slave Clocks is equal to the number of **Delay request messages** received by the emulated Slave Clocks.

   b. If the test run passes (that is, if the DUT is able to handle the presented load), repeat the test with a larger number of emulated slaves. If you have access to the DUT's Command Line Interface (CLI) or Web User Interface (WebUI), you may use the DUT CPU load to more quickly estimate the ultimate slave load.

   c. If the test run fails (that is, if the DUT is not able to handle the presented load), then repeat the test with a smaller number of emulated slaves.

   d. Repeat the test using a **binary search** to find the maximum number of slaves that can be supported by the DUT, to a suggested accuracy of 10%.

Table 4. Binary Search Example – Find the Maximum Number of Slaves that the DUT can Support

Number of Emulated Slaves	Test Run Result	DUT CPU Load
50	Pass	10%
500	Fail	99%
300	Pass	90%
400	Fail	98%
350	**Pass**	97%
375	Fail	98%

5. Repeat the entire test at a few different message rates, as shown in the example table below, to characterize the DUT under a range of conditions.

Table 5. Slave Scalability Results Example – Characterize Scalability Under a Range of Conditions

Sync Rate (messages per second)	Delay-Request Rate (messages per second)	Max # of Slaves
1	1	350
8	8	
32	1	

   a. The Master Clock **Sync message rate** is changed on the DUT using its CLI or WebUI.

b. The emulated Slave Clock **Delay-Request message rate** can be either controlled by the Master Clock (using its CLI or WebUI), or changed on the emulated Slave Clock by setting the **Delay request interval mode** to **Manual** and the **Log minimum delay request interval** to the appropriate value.

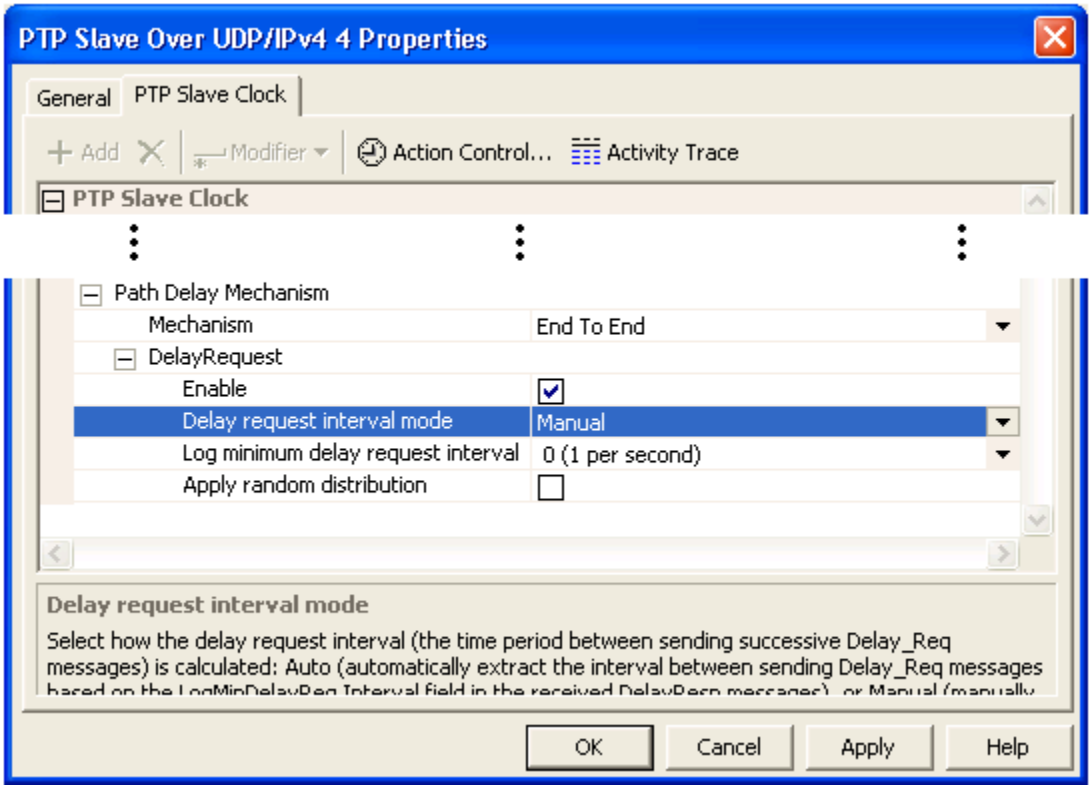


Figure 21. **Set the Emulated Slave Clocks' Delay Request Message Rate**

Test Variables

Repeat the test with the following suggested variations:

- Test with **multiple clock domains**. This will gauge the DUT's scalability while handling multiple domains at the same time.
- Test with two or more Ixia ports, and verify the PTP Slave scalability of the DUT across multiple ports.
- Test with the system in both PTP **multicast** mode and in PTP **unicast** mode.
- Test with the system in both **one-step mode** (which reduces the number of messages) and in **two-step mode**.
- Test with DUT in Master Clock, Boundary Clock, or Transparent Clock modes.
- Add a second Ixia port and send real-world user traffic (Data Plane) between the two Ixia ports. This would test the DUTs ability to maintain maximum PTP scale while forwarding user traffic.

Results Analysis

The results showed how the maximum PTP scalability of the DUT acting as a Master Clock, and how many Slaves it can successfully maintain in a real-world environment.

Conclusions

Confidence in the scalability of each and every system component is vital to the operation of any IEEE1588 system.

Test Case: Best Master Clock (BMC) Selection by Using IxNetwork

Overview

The Best Master Clock (BMC) algorithm is used by Slave Clocks and each Slave port of Boundary Clocks to select the highest quality Master Clock available on the domain. It is a complex algorithm that compares a number of different clock quality parameters, in a specified order of priority, to deterministically select the best available Master.

Testing BMC is important. Incorrect selection can lead to disagreement between slaves as to the best master (leading to different active Master Clocks among Slave Clocks within the same domain), or inappropriate use of a Master Clock of lower quality or one that is intended only as a backup.

IxNetwork can test BMC by emulating multiple Master Clocks with different Clock Quality parameters on one or more test ports. If the DUT is a Boundary Clock, a downstream IxNetwork emulated Slave Clock can be used to easily determine the system's Grandmaster and therefore, the Master Clock selected by the DUT.

Objective

This test verifies that a Boundary Clock or Slave Clock correctly implements the Best Master Clock (BMC) algorithm.

This example describes the setup and steps needed to test a Boundary Clock DUT. If your DUT is a Slave Clock, you will need to verify clock selection using the DUT's own command-line interface (CLI), network management interface, or Web user interface (WebUI).

Setup

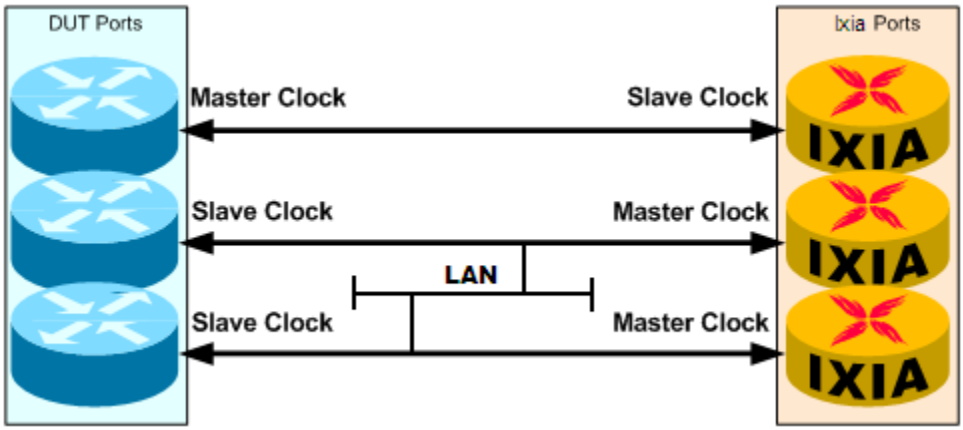


Figure 22. Best Master Clock Selection test setup

Configure the DUT and IxNetwork as follows:

- Configure the DUT as a Boundary Clock with three ports:
  - Two Slave ports (to connect to the two IxNetwork Master ports through a LAN).
  - One Master port (to connect to the IxNetwork slave port).
- Configure IxNetwork with three ports:
  - Two ports will be used as Master ports (each of which will emulate one or more Master Clocks). Connect each IxNetwork Master port to a DUT Slave port through a LAN.
  - One port will be used as a Slave port (which will emulate a Slave Clock). Connect the IxNetwork Slave port to the DUT Master port.

    The IxNetwork Slave port will enable monitoring of the system's Grandmaster. This will enable us to determine the Master Clock selected by the DUT without the need to query the DUT's CLI or WebUI.

Step-by-Step Instructions

1. After reserving the three IxNetwork test ports, start the **PTP Wizard** by double-clicking **PTP**.

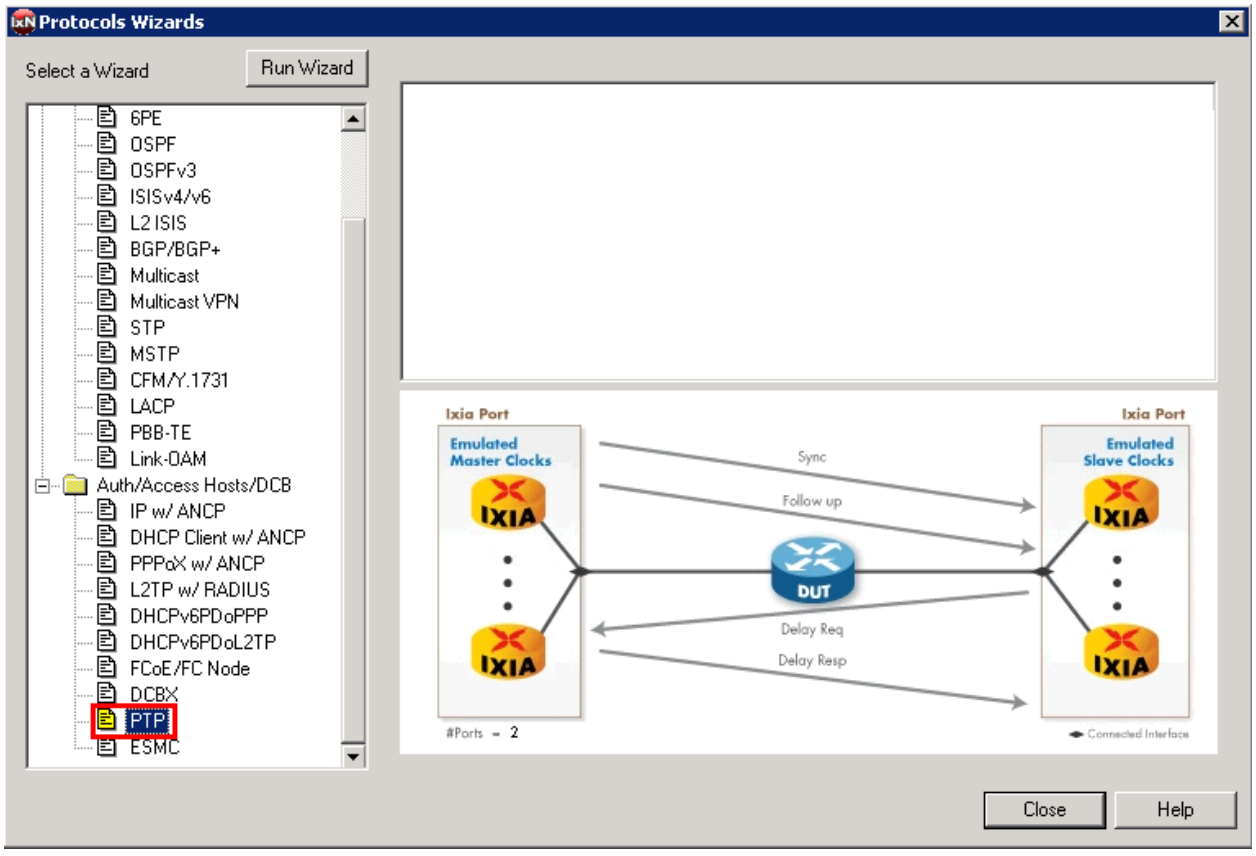


Figure 23. PTP Wizard - Initial Screen

2. On the first page of the PTP wizard, configure key PTP settings and the role of the IxNetwork tests port(s). The 'PTP Scenario' defaults shown are common with many PTP devices, however, ensure that they match the DUT, or the Slaves may not be able to communicate with the Master.

   a. Change the **Role** of both Master ports to *Master*.

   b. Optionally, use the lists on the other options to change key PTP settings.

   Note: The wizard can only configure one *Role* at a time, so if Masters and Slaves are needed in the test, at least two runs of the wizard are required.

   Note: The **Communication Mode** of *Multicast* is used in this test so that the DUT Slave ports can 'choose' the Best Master Clock (over the shared LAN network)

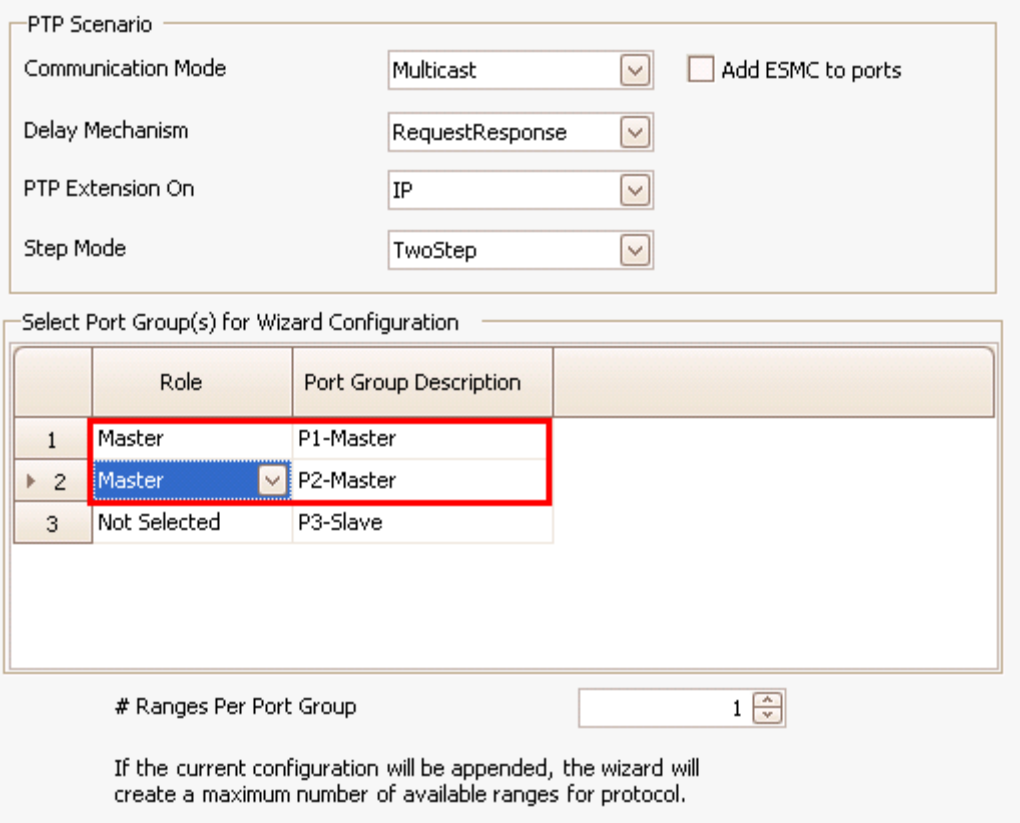


Figure 24. **PTP Wizard – Page 1**

3. The second page of the PTP wizard (mainly) configures the addressing (of the slaves), and the quantity of slaves. Note that IPv6 is also supported.

    a. Change the IP addressing, as required. If the Master and Slaves will be on the same Subnet and there will be many Slaves, it may be required to configure a **Mask** less than */24* (for example use */16*).

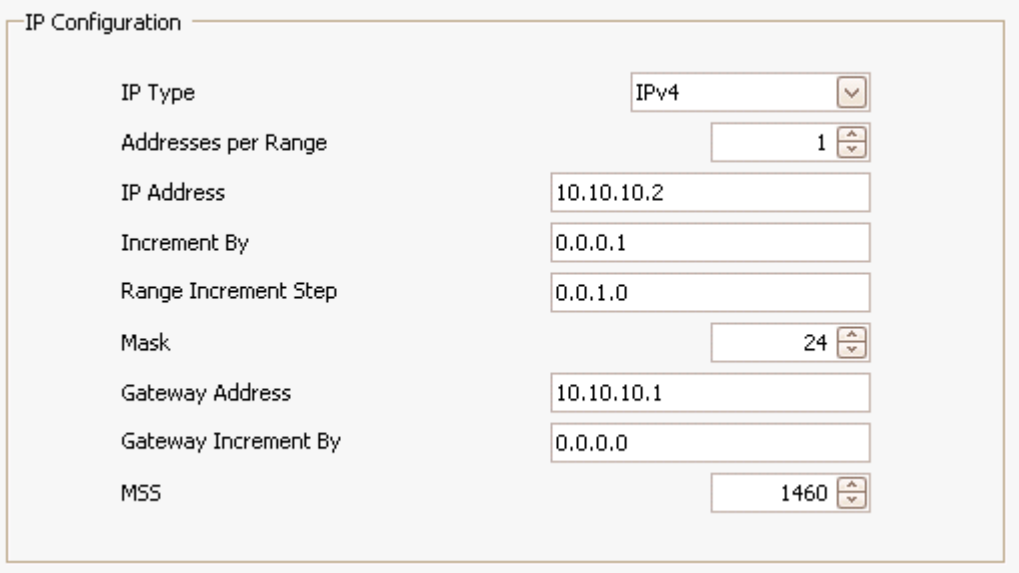


Figure 25. **PTP Wizard – Page 2**

4. The third page of the PTP wizard configures the **Clock Identity** and **Best Master Clock Settings** of the Masters. The Slaves will choose the 'Best Master' based on these parameters. The parameters can also be configured post-wizard. This page also serves to configure **Negative Testing**.
   At the bottom of the page are some of the **Best Master Clock Settings**. This wizard was run with two Master Ports, so both master ports will get these same parameters. Post wizard changes can be made so each Master (range) can have unique BMC settings.

a. Select the **Use Clock Identity** check box and configure the Master Clock Identities as shown. This will make it easier to see the Master that is chosen by the Slaves in the Best Master Clock selection.

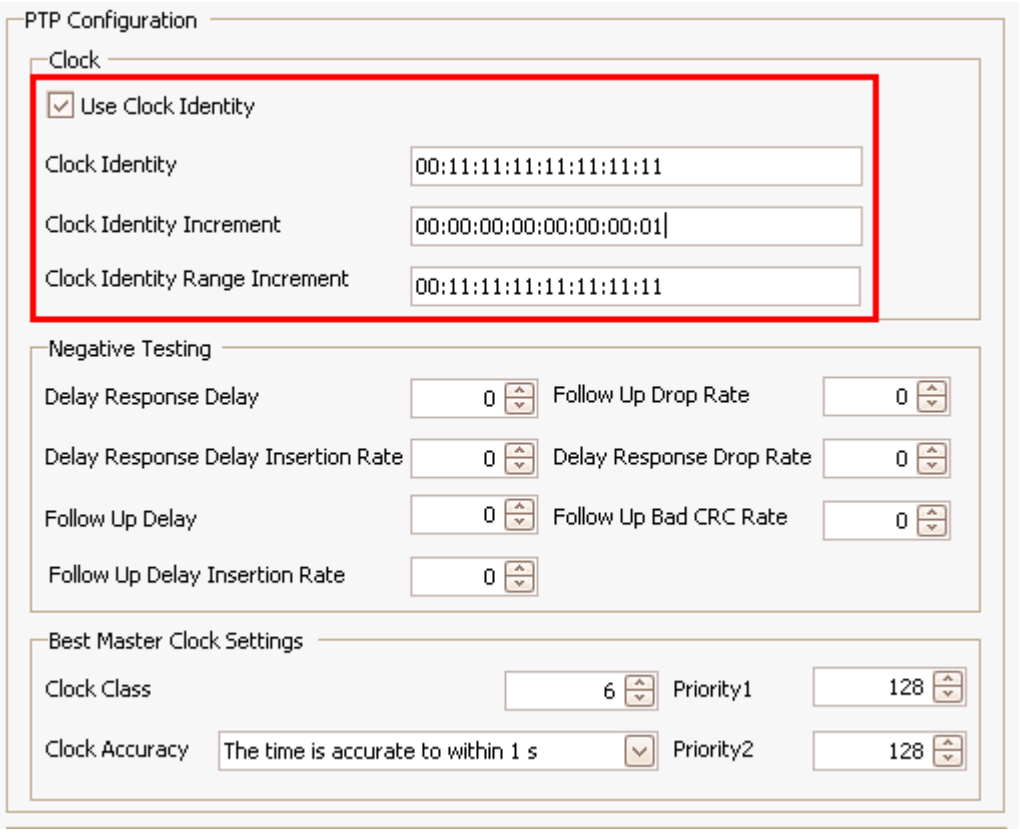


Figure 26. **PTP Wizard – Page 3**

5. The fourth page of the PTP wizard configures the MAC addresses of the Masters.
   a. (Optional) Configure the MAC address of the First, Increment, and Range Increment of the Masters.

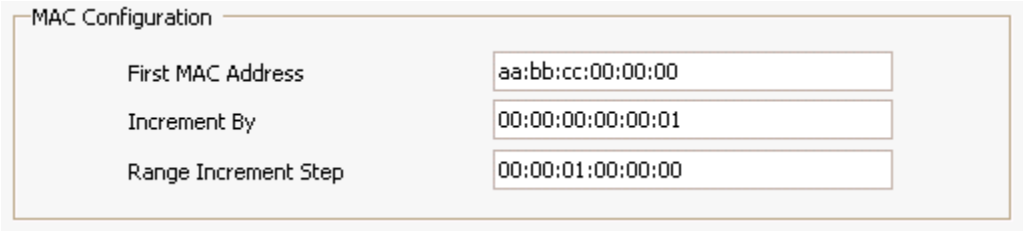


Figure 27. **PTP Wizard – Page 4**

6. The fifth page of the PTP wizard adds VLANs.
   a. (Optional) Select the **Enable Outer** and **Enable Inner**check boxes.

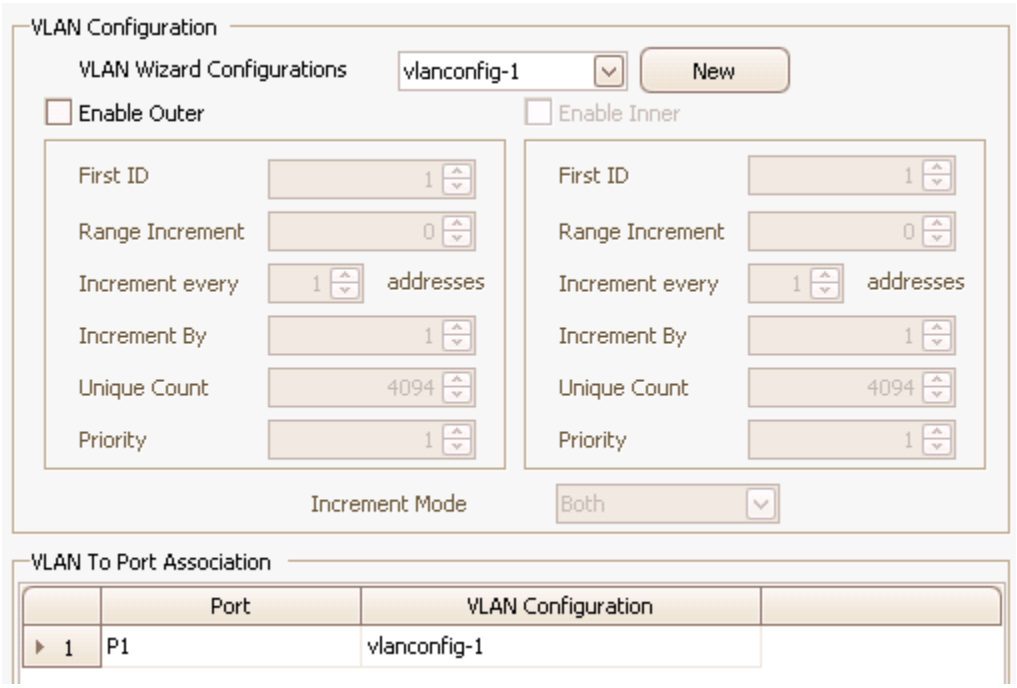


Figure 28. **PTP Wizard – Page 5**

7. On the sixth, and last page of the PTP wizard, configure a **Name** for the parameters just used in this wizard, and select how to apply those parameters.
   a. Configure a name, such as *BlackBook PTP BMC Test Case - Masters*.
   b. Click **Generate and Overwrite** and select the **Identical Protocol stacks** option. This will overwrite any PTP stacks already configured on port *P1-Master and* port *P2-Master.*

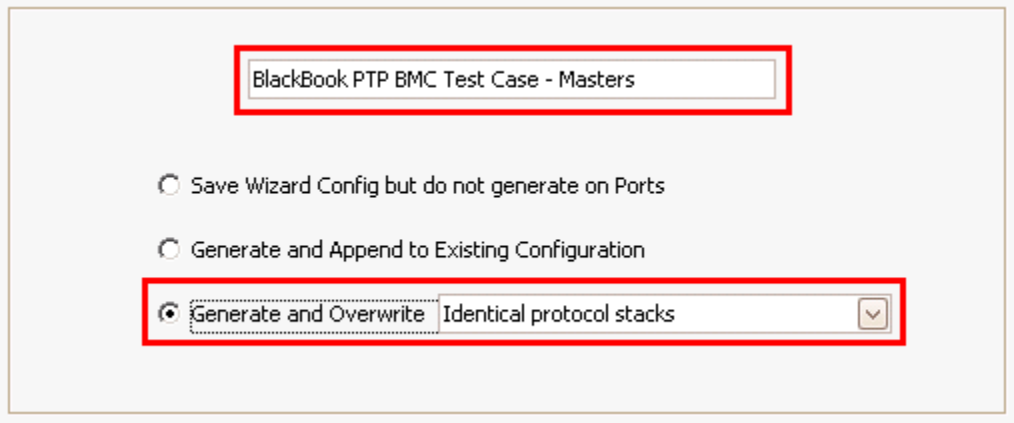


Figure 29. **PTP Wizard – Page 6**

8. After clicking **Finish**, run the PTP wizard again for the slave port by double-clicking PTP.

9. See the Wizard steps for the Slaves as shown in the PTP **Test Case: PTP Scalability using IxNetwork**. Here is a short list of items to change from their defaults for this test case:

    a. Wizard Page 1
        i. Change *P3-Slave* port **Role** to *Slave.*
        ii. Optional: Leave ranges at 1.
    b. Wizard Page 2
        i. Optional: Change **Addresses per Range** to *5.*
        ii. Change IP addresses, as required.
    c. Wizard Page 3
        i. Optional: Change **Clock Identity** to unique value. Ensure that they are different from the Masters wizard run.
    d. Wizard Page 4
        i. Change **First MAC Address** to something unique. Ensure that they are different from the Masters wizard run.
    e. Wizard Page 5
        i. Optional: Add VLAN config.
    f. Wizard Page 6
        i. Save Wizard as *BlackBook PTP BMC Test Case – Slaves.*
        ii. Click **Generate and Overwrite**.

10. After clicking **Finish**, close the wizard and view the wizard configuration in the main IxNetwork GUI.
    a. Go to **Auth/Access Hosts/DCB -> Static IP/w/Auth -> Static IP -> PTP** to see the two Master ports and one Slave port configurations that was created.

    b. Note the **First Clock** Clock Identity of each Master. This will be needed to understand the Best Master Clock Selection in the statistics.

    c. (Optionally) Scroll to the right to view or change the settings of each range.

d. (Optionally) Click the **IP** or **MAC** tabs at the bottom to see the lower layer configuration.

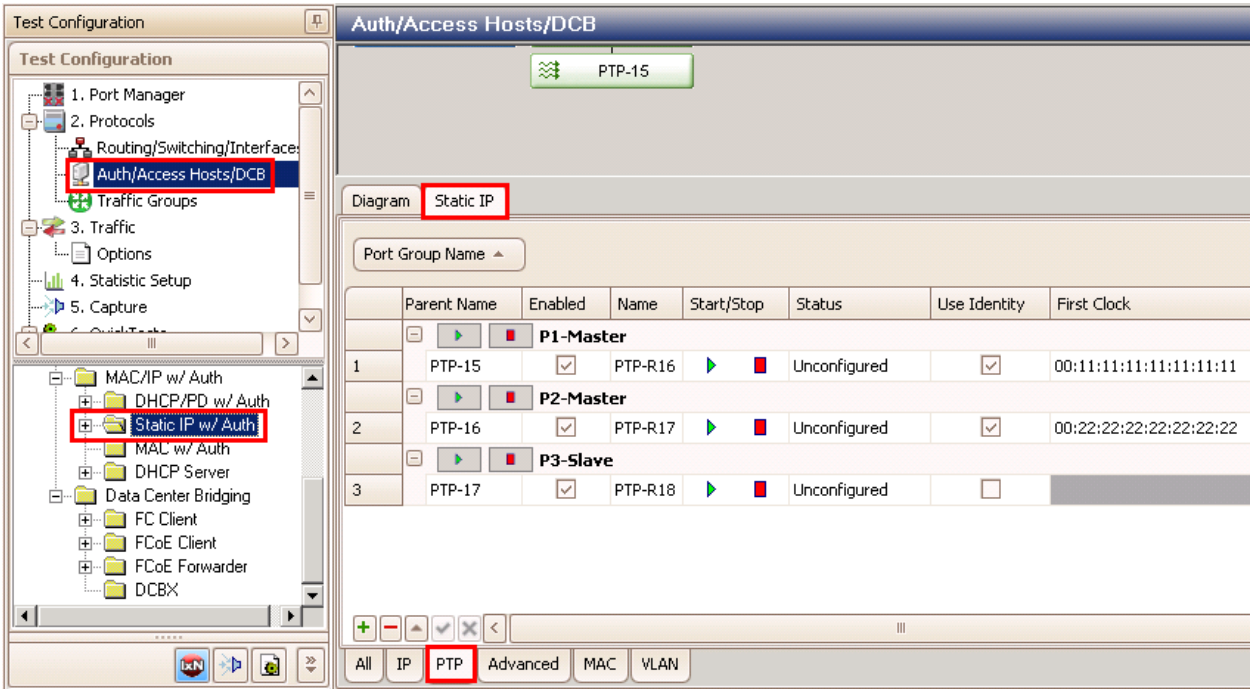


Figure 30. **Post Wizard PTP Configuration Screen**

11. Start the PTP Emulation.
    a. Start the PTP emulation by clicking the green arrow button(s). The left green button will start all the ranges on the port, and the right green buttons will start one range at a time (in this case, there is only one range per port). The **Status** column should change to *Negotiated when* the PTP protocol is running on the Ixia port(s).

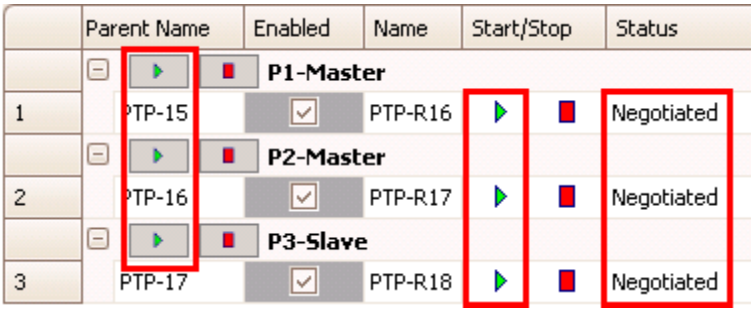


Figure 31. **Start PTP Protocol**

12. View the Statistics of the PTP emulation, verifying which BMC was selected by the slaves.
    a. On the lower left of the main IxNetwork window, click **Statistics**  .
    b. Open the **Protocol Summary** and **PTP Per Session** statistics.
        i. To open the **PTP Per Session** statistics, right-click **Protocol Summary** and select **Drill Down per Session.**
    c. Notice that the Slaves have chosen the Master on port *P1-Master* to be its Master Clock. Currently, both Masters have the same BMC settings in the configuration, but *P1-Master* has a lower Clock Identity (*00:11:11:11:11:11:11:11)* so it has been chosen as the Master.
    d. Notice that *P2-Master* has a status of *Passive* because in this Multicast environment, only one Master can be active at a time.

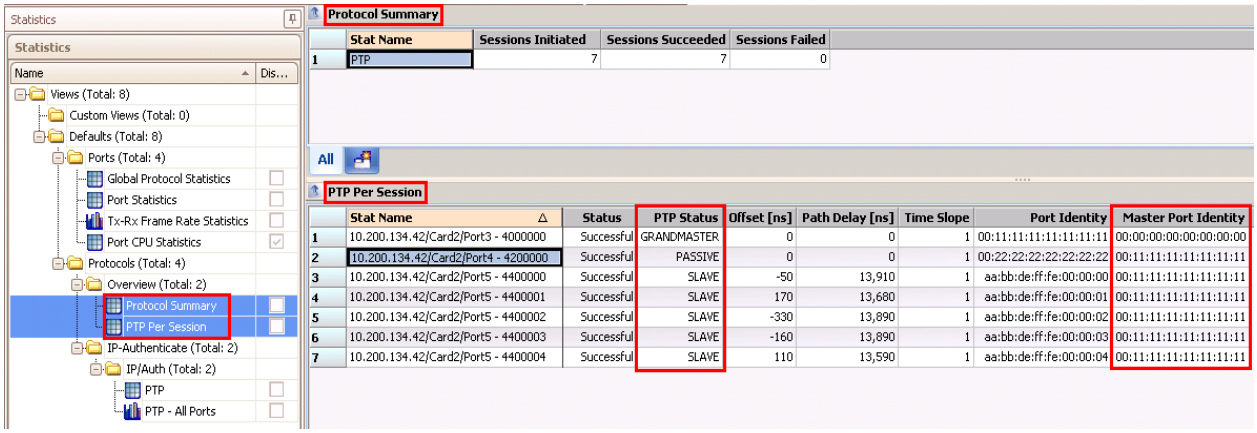


Figure 32. PTP Per Session Statistics

13. Continue the test to verify that the DUT correctly implements and prioritizes other **Best Master Clock** parameters, and that the Slaves follow these changes:
    a. Go back to the **Test Configuration** window. Change port *P2-Master* to be more preferred than the *P1-Master* by setting a higher **Priority 1** value. If this value was at its default of 128, set it to *129.*

b. Observe the statistics. The Slaves have selected port *P2-Master* to be their GrandMaster Clock.

PTP Per Session

	Stat Name	Status	PTP Status	Offset [ns]	Path Delay [ns]	Time Slope	Port Identity	Master Port Identity
1	10.200.134.42/Card2/Port3 - 200000	Successful	PASSIVE	0	0	1	00:11:11:11:11:11:11:11	00:22:22:22:22:22:22:22
2	10.200.134.42/Card2/Port4 - 400...	Successful	GRANDMASTER	0	0	1	00:22:22:22:22:22:22:22	00:00:00:00:00:00:00:00
3	10.200.134.42/Card2/Port5 - 600000	Successful	SLAVE	-50	13,870	1	aa:bb:de:ff:fe:00:00:00	00:22:22:22:22:22:22:22
4	10.200.134.42/Card2/Port5 - 600001	Successful	SLAVE	170	13,790	1	aa:bb:de:ff:fe:00:00:01	00:22:22:22:22:22:22:22
5	10.200.134.42/Card2/Port5 - 600002	Successful	SLAVE	-120	13,820	1	aa:bb:de:ff:fe:00:00:02	00:22:22:22:22:22:22:22
6	10.200.134.42/Card2/Port5 - 600003	Successful	SLAVE	-160	13,790	1	aa:bb:de:ff:fe:00:00:03	00:22:22:22:22:22:22:22
7	10.200.134.42/Card2/Port5 - 600004	Successful	SLAVE	-60	13,740	1	aa:bb:de:ff:fe:00:00:04	00:22:22:22:22:22:22:22

Figure 33. PTP Per Session Statistics

14. Change other **Best Master Clock** parameters. See if the Slaves properly switches to the new Master. Examples include the following:

    a. Configure the *P1-Master* with a higher **Priority 2** value.

    b. Configure the *P2-Master* with a higher **Clock Class** value.

    c. Configure the *P1-Master* with a higher **Timestamp Offset** value.

    d. Configure the *P2-Master* with a higher **Timestamp Offset Variation** value.

    e. Configure the *P1-Master* with a higher **Time source** value.

15. Verify the DUT's ability to select the next-best Master Clock when the current Master Clock fails (also known as **BMC failover**).

    a. Disable the IxNetwork emulation of the currently running best Master Clock (that is, the current Grandmaster, as seen by the Slave Clock) by clicking the red stop button as seen in step 11.

    b. Verify that the DUT reverts to the next-best emulated Master Clock by observing a change in the **PTP Per Sesssion** statistics.

16. (Optional) Additional **per range/session** statistics can be added to the statistics view.

    a. Hover the mouse over the **PTP Per Session** as shown in the following image, click the **Filter/Sort** list, and then add the required statistics.

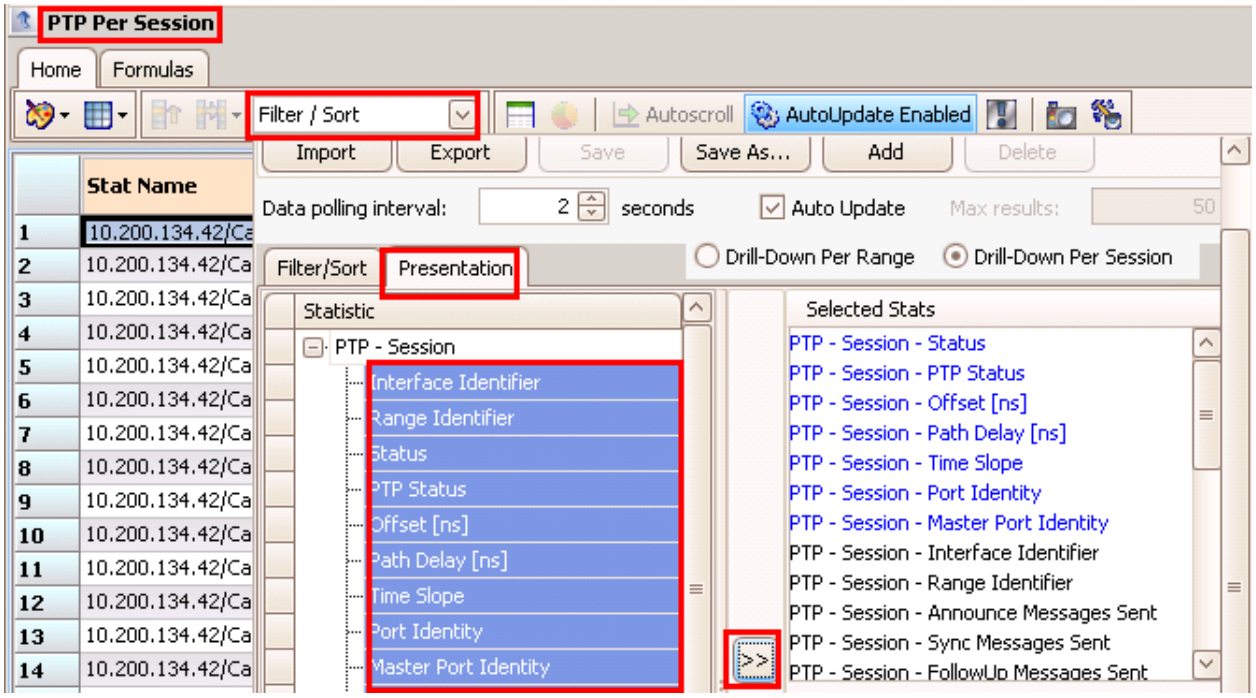


Figure 34. **Adding more PTP Statistics**

17. For additional troubleshooting and validation of PTP elements, use the capture/analyzer tool.

    It can automatically filter out unrelated protocol messages, providing a clear trace of the conversations between PTP endpoints, in real time. The tool captures both incoming and outgoing PTP messages, with on-the-fly filters to quickly find a specific packet.
    The Expanded Decode of the PTP packet (DelayRequest message) is shown in the following figure.

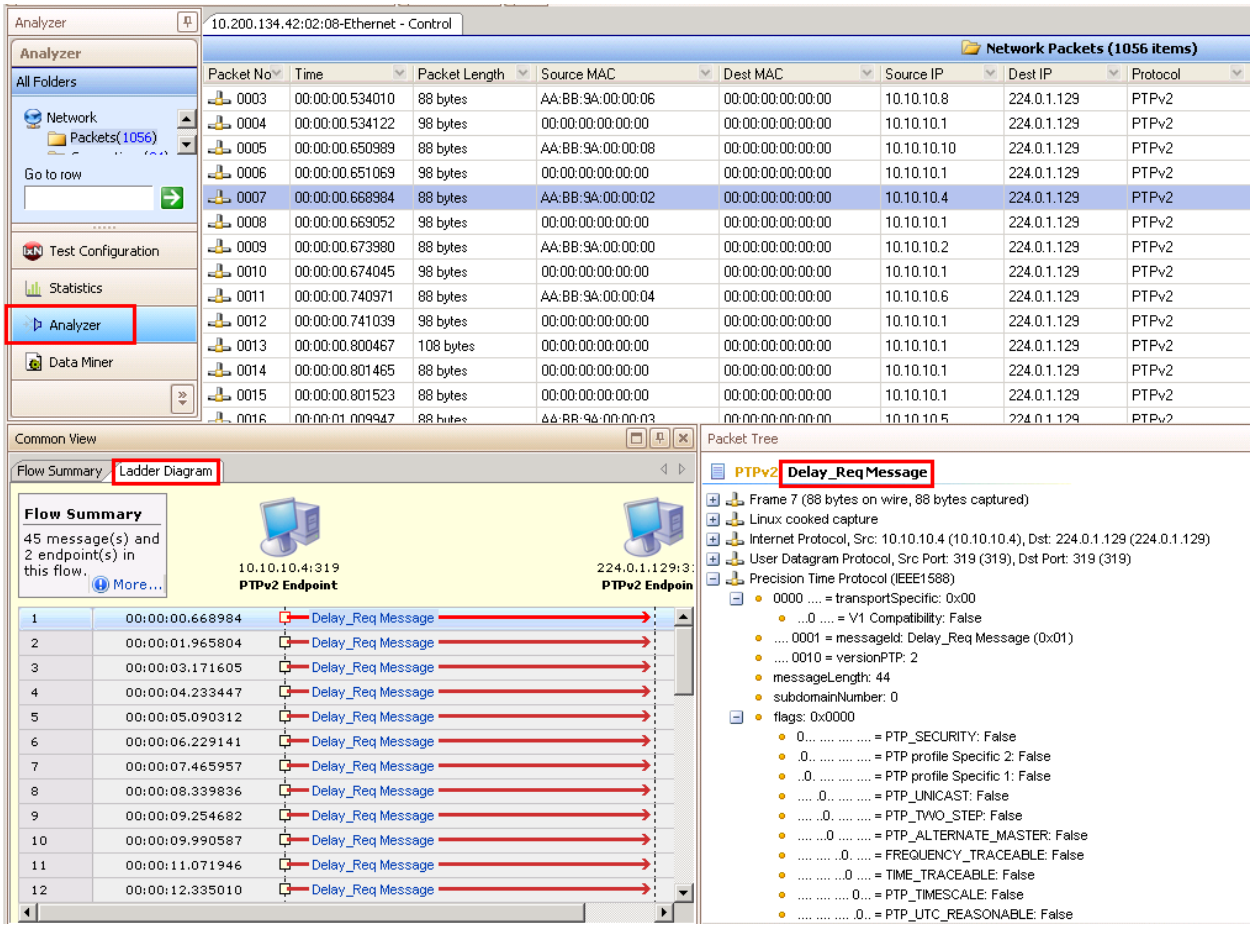


Figure 35. **IxNetwork Analyzer – PTP Decodes**

Test Variables

Repeat the test with the following suggested variations:

- Use combinations of two or more **Clock Quality** parameters on the IxNetwork emulated Master Clocks, configured with conflicting priorities, to test the DUT's prioritization of those parameters. For example, set one parameter (the **Priority 1** parameter) to a higher value on Master Clock 1, and a different parameter (**Priority 2**) to a higher value on Master Clock 2.
- Test with both the DUT and the tester in PTP multicast mode and in PTP unicast mode.
- Test with multiple Master Clocks emulated on **multiple IxNetwork Master ports**, to test the DUT's ability to correctly use the BMC algorithm across multiple DUT ports, multiple DUT line cards, and multiple DUT shelves or racks. This will require additional IxN2X test ports and additional DUT Slave ports.

Results Analysis

Compare the results of the test with the IEEE standard, which specifies the BMC algorithm (see Figures 27 and 28 on pages 89-90 of IEEE1588-2008).

Conclusions

Confidence in Best Master Clock selection is vital to the operation of any IEEE1588 system.

Test Case: Best Master Clock (BMC) Selection by Using IxN2X

Overview

The Best Master Clock (BMC) algorithm is used by Slave Clocks and each Slave port of Boundary Clocks to select the highest quality Master Clock available on the domain. It is a complex algorithm that compares a number of different clock quality parameters, in a specified order of priority, to deterministically select the best available Master.

Testing BMC is important. Incorrect selection can lead to disagreement between slaves as to the best master (leading to different active Master Clocks among Slave Clocks within the same domain), or inappropriate use of a Master Clock of lower quality or one that is intended only as a backup.

IxN2X can test BMC by emulating multiple Master Clocks with different Clock Quality parameters on one or more test ports. If the DUT is a Boundary Clock, then a downstream IxN2X emulated Slave Clock can be used to easily determine the system's Grandmaster and therefore the Master Clock selected by the DUT.

Objective

This test verifies that a Boundary Clock or Slave Clock correctly implements the Best Master Clock (BMC) algorithm.

This example describes the setup and steps needed to test a Boundary Clock DUT. If your DUT is a Slave Clock, you will need to verify clock selection using the DUT's own command-line interface (CLI), network management interface, or Web user interface (WebUI).

Setup

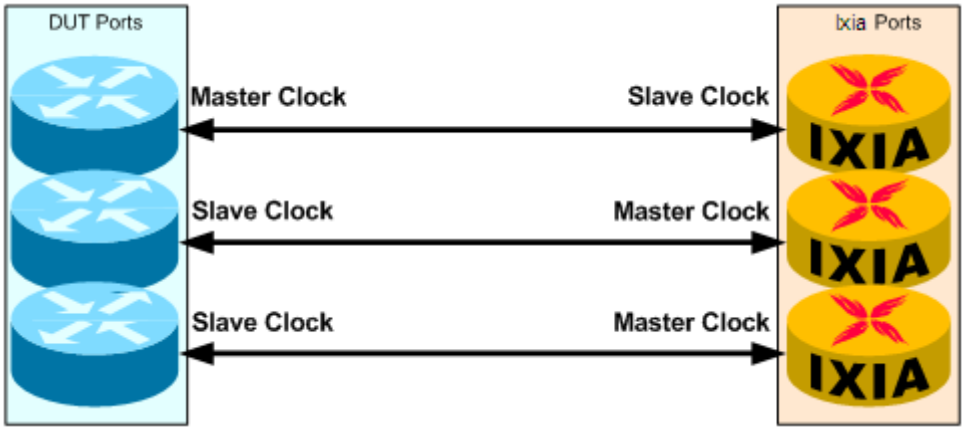


Figure 36. **Best Master Clock Selection test setup**

Configure the DUT and IxN2X as follows:

- Configure the DUT as a Boundary Clock with three ports:
  - Two Slave ports (to connect to the two IxN2X Master ports).
  - One Master port (to connect to the IxN2X slave port).
- Configure IxN2X with three ports:
  - Two ports will be used as Master ports (each of which will emulate one or more Master Clocks). Connect each IxN2X Master port to a DUT Slave port using an Ethernet cable.
  - One port will be used as a Slave port (which will emulate a Slave Clock). Connect the IxN2X Slave port to the DUT Master port using an Ethernet cable.

    The IxN2X Slave port will enable monitoring of the system's Grandmaster. This will enable us to determine the Master Clock selected by the DUT without the need to query the DUT's CLI or WebUI.

Step-by-Step Instructions

1. Configure the IP addresses of the two Master ports and one Slave port of the IxN2X and of the corresponding DUT ports in a similar manner to step 2 of test case **PTP Test Case: Correction Factor Error by using IxN2X**, but with an additional DUT slave port and an additional corresponding IxN2X port for the second Master port.

2. Create an IxN2X Master Clock emulation on Master port 1 with default parameters.

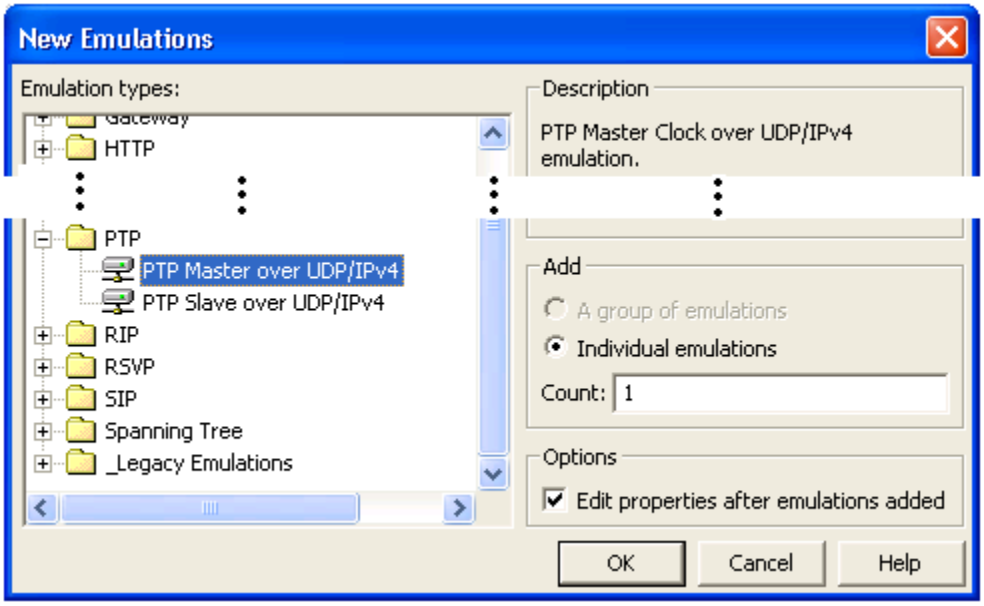


Figure 37. Create a Master Clock Emulation

   a. In the main Setup Emulation window, select the port to be used as Master port 1, and click **New**. Open the **PTP** emulation type, select the **PTP Master over UDP/IPv4** emulation type, check **Edit Properties after emulations added**, and press **OK**. The **Master over UDP/IPv4 Properties** dialog will open.

   b. In the **Master over UDP/IPv4 Properties** dialog, ensure that the **Alternate master flag** is unchecked.

c. Note the **Clock ID** and **Clock Quality** parameters. You will need these later. You may close the dialog by pressing **OK**.

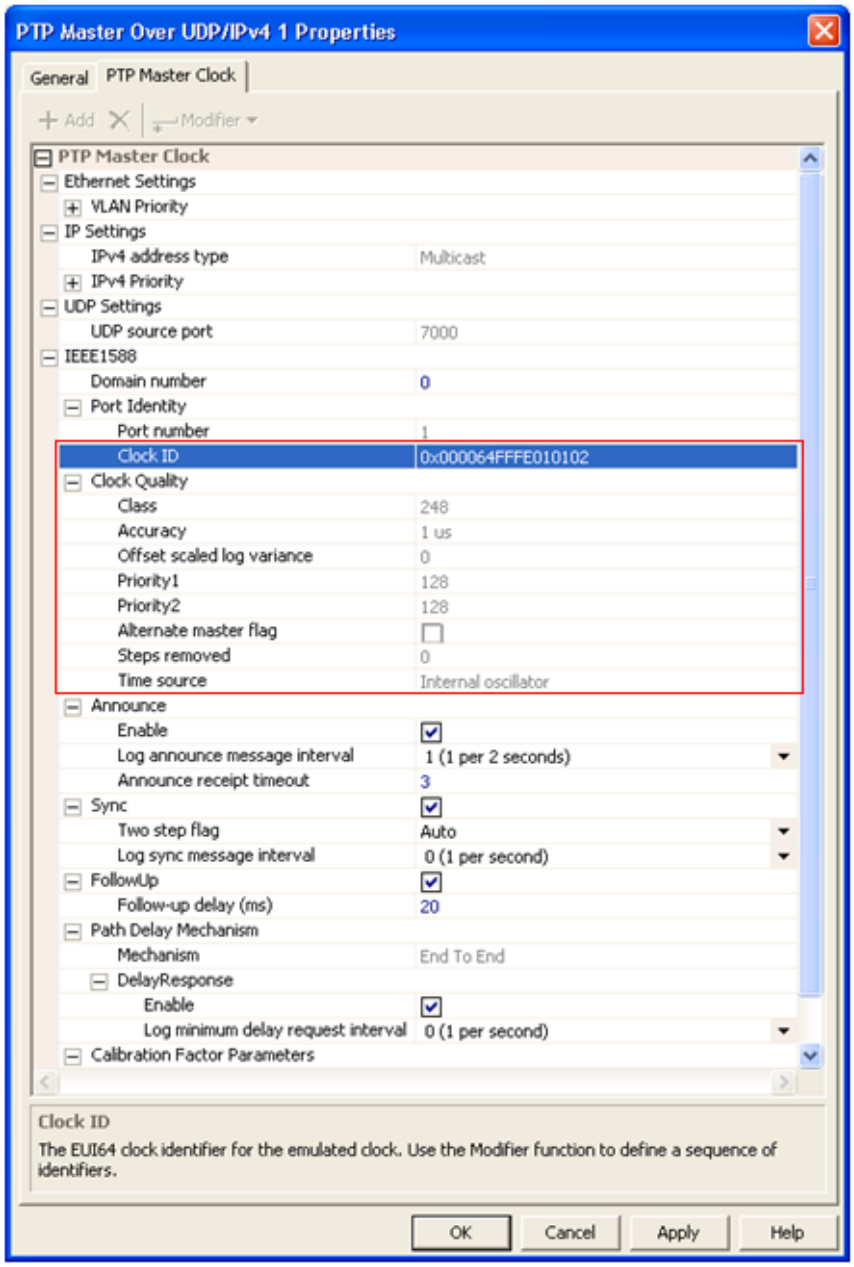


Figure 38. **Note the Clock ID and Clock Quality Parameters**

3. Create a Slave Clock on the Slave port of the IxN2X with default parameters using the same procedure as the previous step, but this time, select the **PTP Slave over UDP/IPv4** emulation type.

4. Enable both devices and verify that the emulated Slave Clock is seeing the emulated Master Clock as the Grandmaster.

a. Check the emulation checkboxes on the main IxN2X **Setup – Emulation** window, to the left of the emulation names, for both the emulated Master Clock and Slave Clock. This enables the IEEE1588 device emulations.

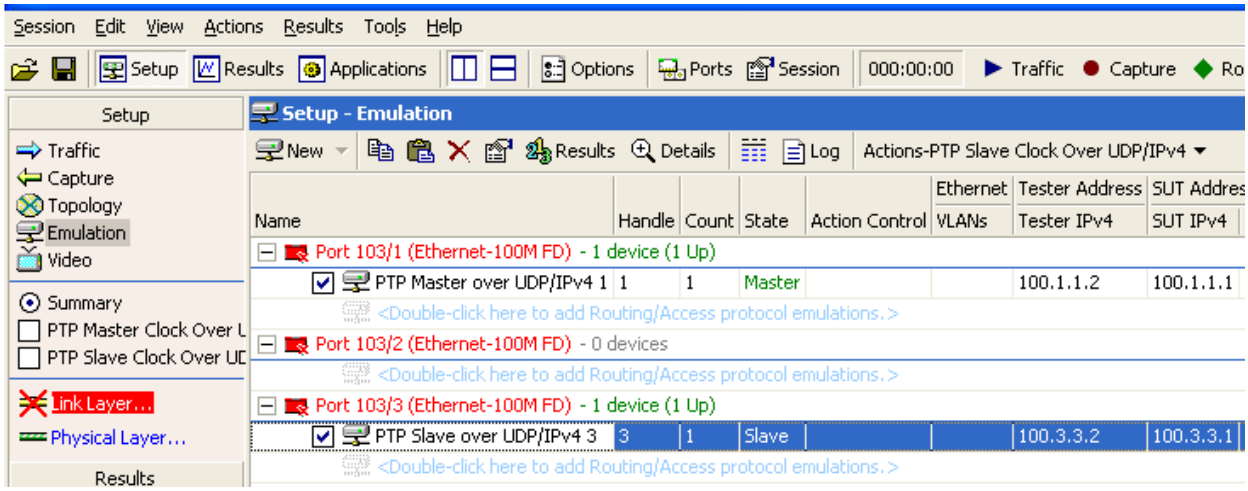


Figure 39. **Verify that the Emulations have Reached the Master and Slave States**

b. Wait for the IxN2X Master Clock and Slave Clock emulations to reach the Master and Slave states, respectively. You can observe the emulation states on the main **Setup – Emulation** window.

c. On the IxN2X main **Setup – Emulation** window, right-click the slave emulation and select **View Details**. This will open the **Slave Instances** dialog. In this dialog, you should see a single row which displays the details of the single slave clock emulation.

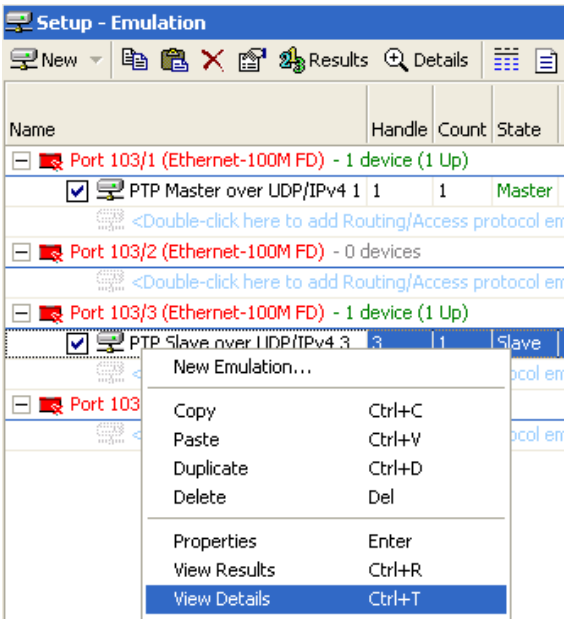


Figure 40. **Right-click the Emulation to View the Slave Instance Details**

d. Double-click this row to open the **Slave Instance Details** dialog. Scroll down to the **Best Master Clock** section. (You may verify these details using the DUT's own CLI or WebUI). Note the DUT's **Grandmaster clock ID** and **Clock Quality** parameters, and verify that these are the same as the **Clock ID** and **Clock Quality** parameters of the Master Clock emulation on IxN2X Master port 1, as noted earlier.

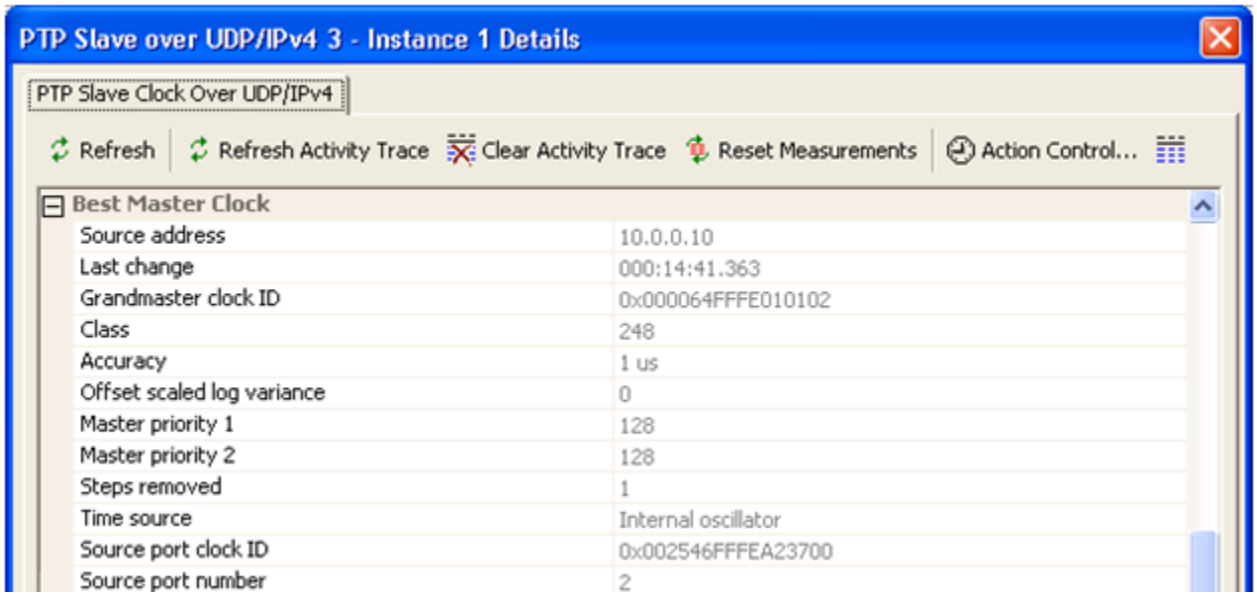


Figure 41. View the Grandmaster Clock ID and Clock Quality Parameters

5. Create and enable a second IxN2X Master Clock.

   a. Create a second emulated Master Clock using the same procedure as Step 2, this time on Master port 2 of the IxN2X.

   b. Note the **Clock ID**. You will use this later.

   c. Ensure that the **Alternate master flag** is unchecked.

d. Change the **Clock Quality** attributes to be better than the **Clock Quality** of Master port 1. (Refer to the IEEE1588-2008 standard, Figures 27 and 28 on pages 89-90). For example, set the **Priority 1** field of the second Master Clock emulation to a lower numerical value (which reflects a higher priority and therefore a better clock). Click **OK** to close the dialog.

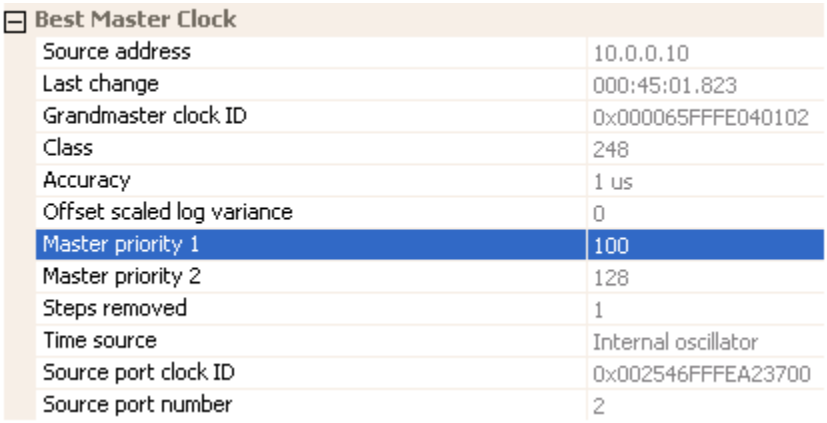


Figure 42. **Change the Priority 1 Field of the Second Master to a Lower Value (Higher Quality)**

e. Enable the Master Clock 2 emulation by checking the emulation checkbox on the main IxN2X **Setup – Emulation** window, to the left of the emulation name.

6. Refresh or re-open the **Slave Instance Details** dialog and observe the value of the **Grandmaster clock ID**. Verify that this has changed to the **Clock ID** of the second Master Clock.

7. Continue the test to verify that the DUT correctly implements and prioritizes the other **Clock Quality** parameters, by creating a series of additional IxN2X Master Clock emulations on Master ports 1 and 2. Create each new emulation on the IxN2X Master port that is not currently the Grandmaster, to enable the change to be observed by viewing a changed **Grandmaster clock ID** in the **Slave Instance Details** dialog. For example:

   a. Create a Master on Master port 1 with a higher **Class** parameter.

   b. Create a Master on Master port 2 with a higher **Accuracy** parameter.

   c. Create a Master on Master port 1 with a higher **Offset scaled log variance** parameter.

   d. Create a Master on Master port 2 with a higher **Priority 1** parameter.

   e. Create a Master on Master port 1 with a higher **Priority 2** parameter.

   f. Create a Master on Master port 2 with a higher **Steps Removed** parameter.

   g. Create a Master on Master port 1 with a higher **Time source** parameter.

8. Verify the DUT's ability to select the next-best Master Clock when the current Master Clock fails (known also as **BMC failover**).

    a. Disable the IxN2X emulation of the best Master Clock (i.e., the current Grandmaster, as seen by the Slave Clock) by clearing the checkbox to the left of the appropriate emulation within the IxN2X **Setup – Emulation** dialog. (If you have run all the steps above, this will be the last Master Clock created).

    b. Verify that the DUT reverts back to the next-best emulated Master Clock by observing a changed **Grandmaster clock ID** in the **Slave Instance Details** dialog.

Test Variables

Repeat the test with the following suggested variations:

- Use combinations of two or more **Clock Quality** parameters on the IxN2X emulated Master Clocks, configured with conflicting priorities, to test the DUT's prioritization of those parameters. For example, set one parameter (e.g., the **Priority 1** parameter) to a higher value on Master Clock 1, and a different parameter (e.g., **Priority 2**) to a higher value on Master Clock 2.
- Test with both the DUT and the tester in PTP **multicast** mode and in PTP **unicast** mode.
- Test with multiple Master Clocks emulated on **multiple IxN2X Master ports**, to test the DUT's ability to correctly use the BMC algorithm across multiple DUT ports, multiple DUT line cards, and/or multiple DUT shelves or racks. This will require additional IxN2X test ports and additional DUT Slave ports.

Results Analysis

Compare the results of the test with the IEEE standard which specifies the BMC algorithm (see Figures 27 and 28 on pages 89-90 of IEEE1588-2008).

Conclusions

Confidence in Best Master Clock selection is vital to the operation of any IEEE1588 system.

Test Case: Correction Factor Error by Using IxNetwork

Overview

One of the most critical functions of a Transparent Clock (TC) is to correctly measure the **latency** (in ns) experienced by PTP packets as they pass through it. This latency is also known as the **Residence Time**. The TC sends this latency information to downstream PTP entities as a value known as the **Correction Factor**. If the Correction Factor is inaccurate or if Transparent Clock behavior is not implemented within a switch or router, downstream Slave Clocks may not be able to synchronize accurately to the upstream Master.

There have been multiple test methodologies proposed for TC testing. One of the methodologies is discussed here using IxNetwork. Please refer TC test cases in Clock Quality section for other advanced methodologies.

Using IxNetwork, you can measure the actual latency of each PTP packet as it passes through a TC and compare that to the reported Correction Factor. This provides a measure of how well the TC is calculating the Correction Factor.

The Correction Factor error (CF error) is calculated as follows:

CF error = Correction Factor – Actual Latency

Positive values of CF error indicate that the TC is overestimating the residence time, while negative values indicate that it is underestimating.

This CF error metric, which was introduced and demonstrated on the IxNetwork test platform during the ISPCS 2009 Symposium, is recognized as a basic metric of TC performance. Using a TC with large CF errors may result in inaccurate and varying synchronization of downstream Slave Clocks. If the CF errors are large and vary greatly, the resulting instabilities may cause downstream Slave Clocks to lose synchronization.

Generally, a Correction Factor error of greater than several tens of nanoseconds is considered significant, however, this depends entirely on the requirements of your application.

Objective

This test measures the Correction Factor Error of either a Transparent Clock or a cascaded series of Transparent Clocks.

This example describes the setup and steps needed to test a single Transparent Clock.

Setup

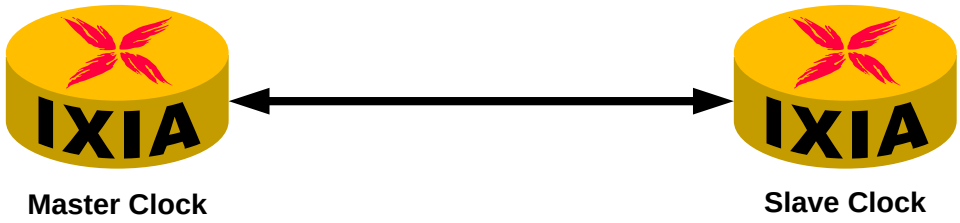


Figure 43. Calibration setup

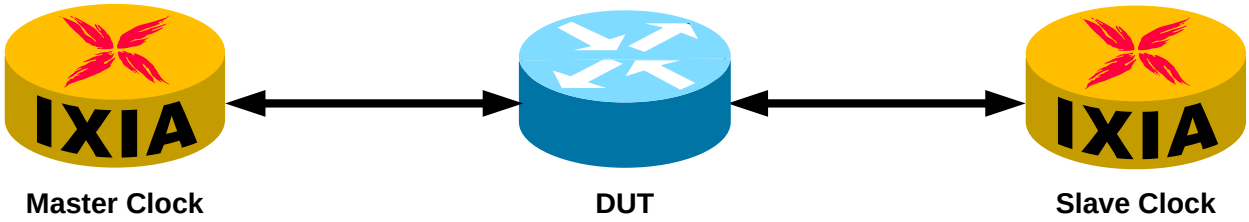


Figure 44. Correction Factor Error test setup

About Calibration

To measure the Correction Factor accurately, ensure that the IxNetwork latency measurement is as accurate as possible, and that the timestamp plane is referenced to actual ingress and egress points of the messages to and from the DUT.

This will help eliminate inaccuracies that may otherwise be caused by the following:

- Internal offsets within IxNetwork (between the point of insertion of timestamps and the test interface connector).
- The propagation delays within the cables connecting the DUT interfaces to the IxNetwork test interfaces. For example, category 5E electrical cable adds a propagation delay of **5.48 ns/m**, while optical fiber adds a delay of approximately **3.29 ns/m**.

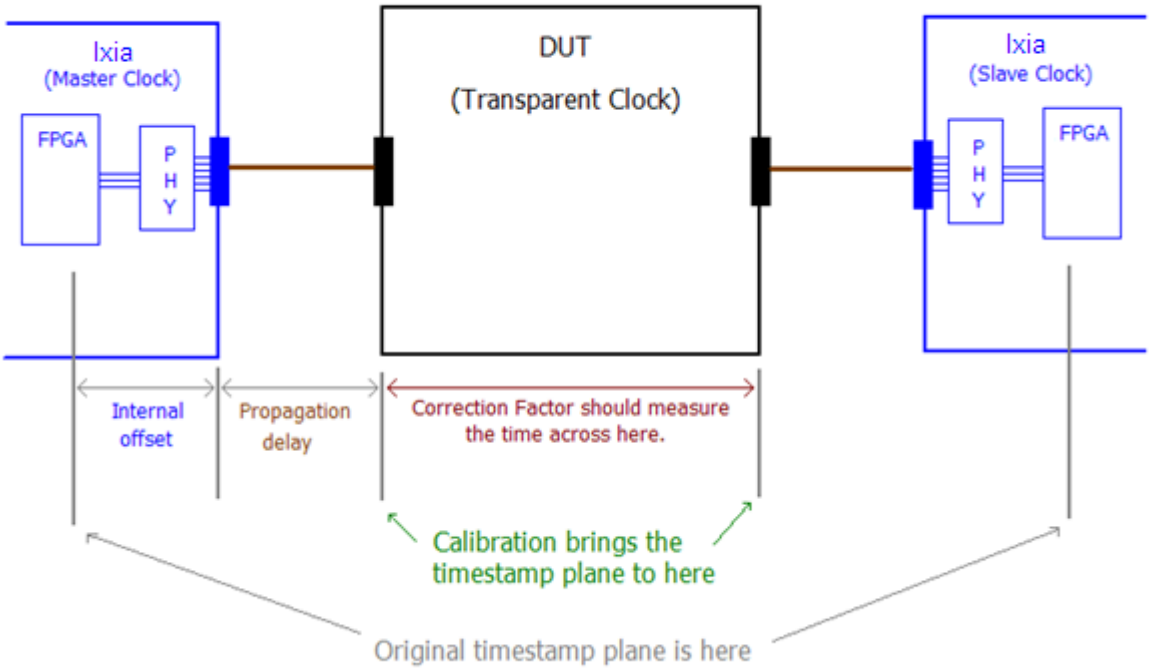


Figure 45. **Calibration helps correct for IxNetwork offsets and cable propagation delays**

While the IxNetwork already has some compensation for internal offsets built into its timestamp engine, it is not able to fully compensate for all aspects of the offsets and cannot automatically take propagation delay into account.

Configurations

There are two configurations for this test:

- **Calibration mode** configuration, for the calibration step, for which we will interconnect two IxNetwork test ports back-to-back using **one Ethernet calibration cable**.
- **Test mode** configuration, for the measurement steps, for which we will connect two IxNetwork test ports to two DUT test ports by using **two Ethernet test cables** of **equal length**.

The length of the calibration cable must be equal to twice the length of one test cable. This is important and will help ensure that there is no contribution to the reported Correction Factor error caused by differing cable lengths.

In summary, you will need three **cables** for this test:

- Two test cables of the same length (**x meters**) to connect the Master test interface to the DUT and to connect the DUT to the Slave test interface during the measurement steps. Measure the length of this cable.

- A calibration cable that is twice as long (**2x meters**) to connect the Master test interface directly to the Slave test interface during the calibration step.

Calibration mode

- The DUT is not required.
- Configure IxNetwork with two test ports:
  - One test port will be used as Master port (on which we will emulate a Master Clock).
  - One test port will be used as a Slave port (on which we will emulate a Slave Clock).
- Connect the IxNetwork Slave port to the IxNetwork Master port by using the **Ethernet calibration cable**.

Test mode

- Configure the DUT as a Transparent Clock with two ports:
  - One Slave port (to connect to the IxNetwork Master port).
  - One Master port (to connect to the IxNetwork Slave port).
- Configure IxNetwork with two test ports:
  - One test port will be used as Master port (on which we will emulate a Master Clock). Connect the IxNetwork Master port to the DUT Slave port by using **one of the Ethernet test cables**.
  - One test port will be used as a Slave port (on which we will emulate a Slave Clock). Connect the IxNetwork Slave port to the DUT Master port by using **the other Ethernet test cable**.

Step-by-Step Instructions

1. Cable the IxNetworks ports Back-to-Back (See **Setup: Calibration Mode**).

2. Calibrate the timestamps:

   If a calibration cable of the correct length cannot be obtained or constructed, you must still carry out the calibration procedure to account for the internal test equipment residual latencies. You may then use the above cable propagation-delay estimates to either determine or correct for the calibration error that is likely to result from using a calibration cable of incorrect length. Using the calibration cable, run the following steps.

   a. Configure a Master and Slave(s) as per the ***PTP Test Case: Best Master Clock (BMC) Selection by using IxNetwork*.**
   b. Start the protocol emulation. Ensure that the Master/Slave status goes to *Successful.* Note the *Path Delay (ns)* of the Slave(s) after a period of time, after these measurements have settled.

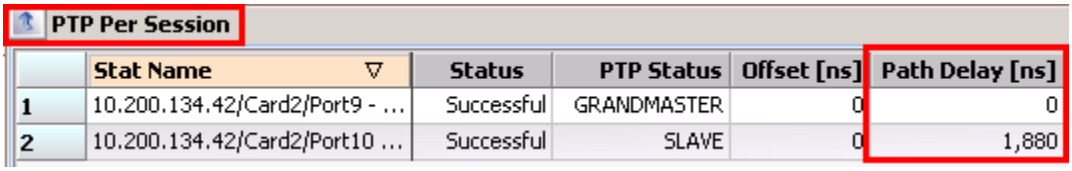


Figure 46. **Viewing the Path Delay of the Slave during Calibration**

3. Stop the Protocol Emulation.
4. Cable the IxNetwork ports to the DUT, with the DUT acting as the Transparent clock (See **Setup: Test Mode**).
5. If necessary, reconfigure the link layer and IP addresses on the IxNetwork Master port and the IxNetwork Slave port, as necessary. An example of this can be seen in the ***PTP Test Case: Best Master Clock (BMC) Selection by using IxNetwork*.**
6. Configure the Master port to be in *Transparent/Master* mode.
    a. Go to **Test Configuration -> Auth/Access Hosts/DCB -> Static IP w/Auth -> Port Group Settings - > Clock role**. Change the *Master* port to T*ransparent/Master.*

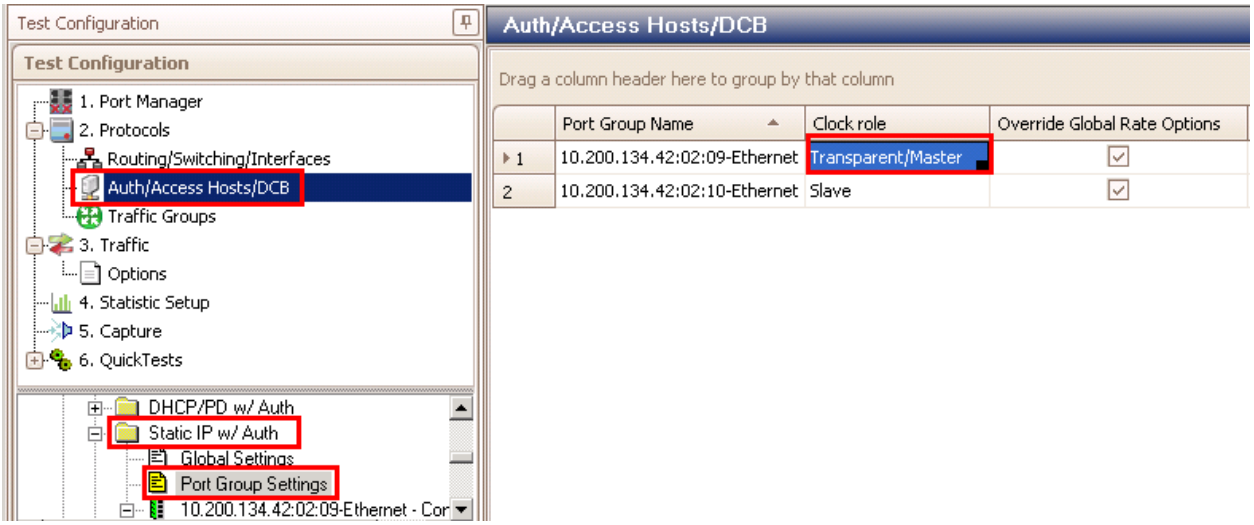


Figure 47. **Configuring the port to be Transparent/Master Clock**

7. Enter the **Path Delay (ns)** value as determined in step 2b, into the **Residence Time** field of the Transparent/Master Clock.

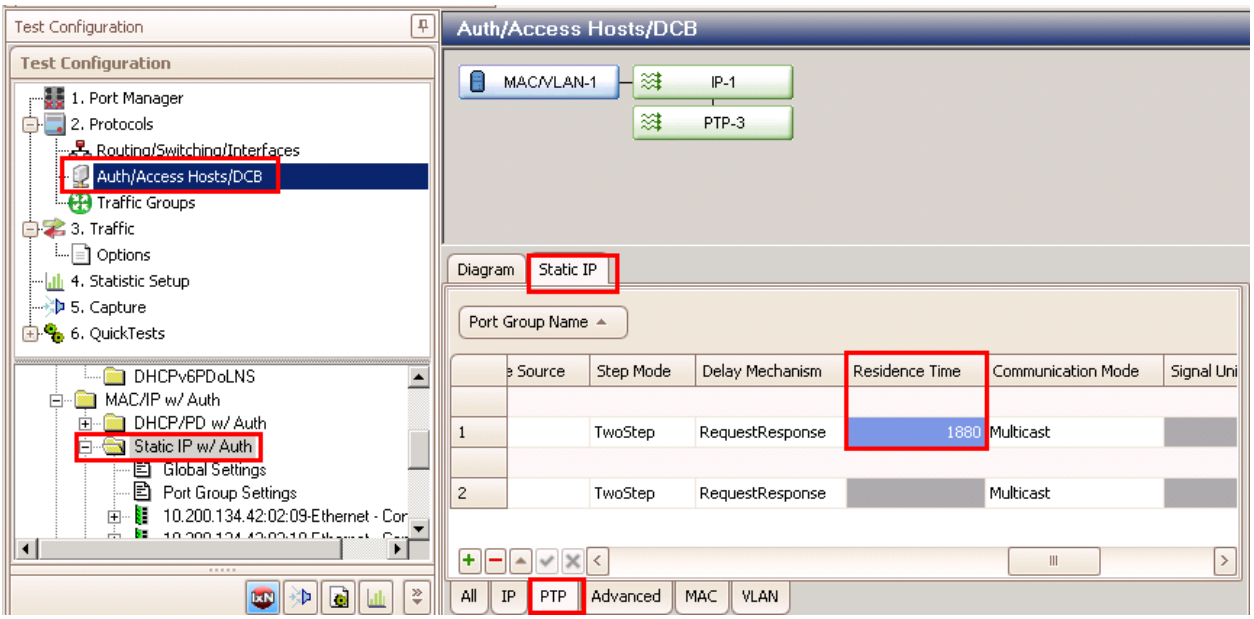


Figure 48. **Configuring Correction Error Residence Time**

8. Start the PTP protocol emulation by clicking **Start All Protocols** on the top toolbar.
9. Measure Correction Factor Error.
   a. Observe the Statistics -> Path Delay (ns).

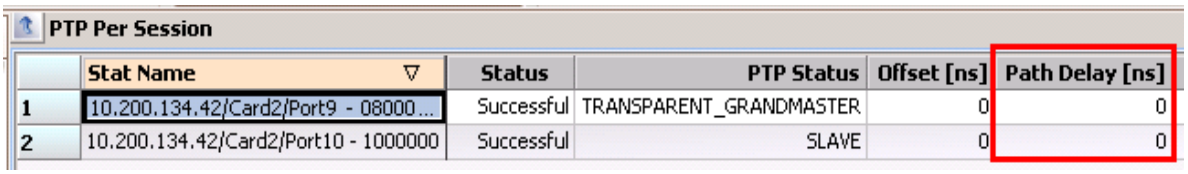


Figure 49. **Measure Correction Factor with DUT**

   b. You may have to adjust the calibration factors slightly to zero out the **Path Delay**, as follows:
      i. Stop the protocol emulation.
      ii. Change the **Residence Time** as explained in Step 7.
      iii. Start protocol emulation again.
      iv. Observe **Path-Delay (ns).**

      Note that the magnitudes of the residual latencies and the stability of the calibrated values will vary according to the type of IxNetwork test card used and the line rate (10/100/1000/10000 Mb/s) used.

After IxNetwork is properly calibrated, the measured **Path Delay (ns)** values will accurately represent the actual PTP packet residence time in the DUT, excluding some small residual

internal IxNetwork offsets (for example, variable PHY delays) and propagation delays in the cables.

Note that the IxNetwork real-time **traffic-based latency** measurements remain unchanged and will be larger than the **PTP emulation Path Delay** measurements.

Test Variables

Repeat the test with the following suggested variations:

- Increase the Sync/Delay Request **message rates,** as required.
- Increase the **number of slaves** emulated on the slave port to 100, depending on the expected load in the target system. (See also ***PTP Test Case: PTP Scalability by Using IxNetwork***).
- Run the test across **different pairs of ports**, across port pairs in **both directions** at the same time (by using different clock domains), and across **multiple port pairs** at the same time. We recommend this because port asymmetries and unexpected performance differences have been found in at least one commercial Transparent Clock, and because testing on multiple port pairs at the same time may load the DUT and impact the Correction Factor accuracy.
- Run the test on **multiple clock domains** simultaneously. This will test whether the Transparent Clock DUT is able to be syntonized to multiple upstream Master Clocks (on different clock domains) at the same time. A lack of syntonization of the Transparent Clock will cause its time base (for CF calculations) to be inaccurate. This may cause a CF Error result that is higher than expected and increases linearly with increasing forwarding latency.
- Introduce **background data-plane (user) traffic** by creating non-PTP traffic streams to and from the Master and Slave ports.
- Add a **control-plane load**, for example, by emulating the Spanning Tree Protocol (STP) or other protocols, and rapidly changing the protocol parameters or flapping the emulated devices.
- Run the test in both PTP **multicast** mode and PTP **unicast** mode.

Results Analysis

The measured Correction Factor Error should be less than the DUT specification or less than the requirements of the target system or network, under all conditions that might be expected. Generally, the Correction Factor error should be less than a few hundred nanoseconds, however, this varies depending on the application of your DUT.

Conclusions

Correction Factor Error contributes to the time offset experience by each Slave Clock in a system.

The application's timing synchronization requirements will determine the maximum time offset permitted at each Slave Clock. If Transparent Clocks are used in the system, some of this maximum time offset must be budgeted or allocated to Correction Factor Error. **Multiple** Transparent Clocks are likely to be used in a real network, however, so the permitted Correction Factor Error of any single Transparent Clock must be **reduced** according to the maximum number of TCs expected to be **cascaded**.

Test Case: Correction Factor Error by Using IxN2X

Overview

One of the most critical functions of a Transparent Clock (TC) is to correctly measure the **latency** (in ns) experienced by PTP packets as they pass through it. This latency is also known as the **Residence Time**. The TC sends this latency information to downstream PTP entities as a value known as the **Correction Factor**. If the Correction Factor is inaccurate or if Transparent Clock behavior is not implemented within a switch or router, then downstream Slave Clocks may not be able to synchronize accurately to the upstream Master.

There have been multiple test methodologies proposed for TC testing. One of the methodologies is discussed here using IxN2X. Please refer TC test cases in Clock Quality section for other advanced methodologies.

Using IxN2X, you can measure the actual latency of each PTP packet as it passes through a TC and compare that to the reported Correction Factor. This provides a measure of how well the TC is calculating the Correction Factor.

The Correction Factor error (CF error) is calculated as:

CF error = Correction Factor – Actual Latency

Positive values of CF error indicate that the TC is overestimating the residence time, while negative values indicate that it is underestimating.

This CF error metric, which was introduced and demonstrated on the IxN2X test platform during the ISPCS 2009 Symposium, is recognized as a basic metric of TC performance. Using a TC with large CF errors may result in inaccurate and/or varying synchronization of downstream Slave Clocks. If the CF errors are large and vary greatly, the resulting instabilities may cause downstream Slave Clocks to lose synchronization.

Generally, a Correction Factor error of greater than several tens of nanoseconds is considered significant; however, this depends entirely on the requirements of your application.

Objective

This test measures the Correction Factor Error of either a Transparent Clock or a cascaded series of Transparent Clocks.

This example describes the setup and steps needed to test a single Transparent Clock.

Setup

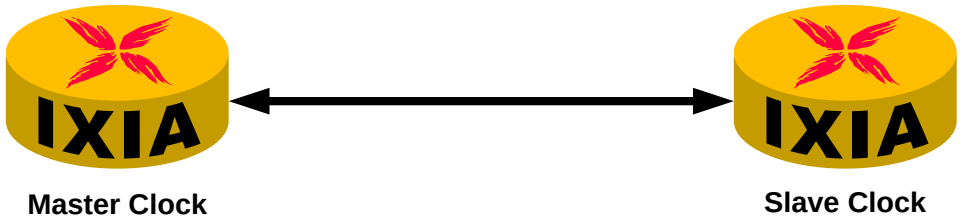


Figure 50. Calibration setup

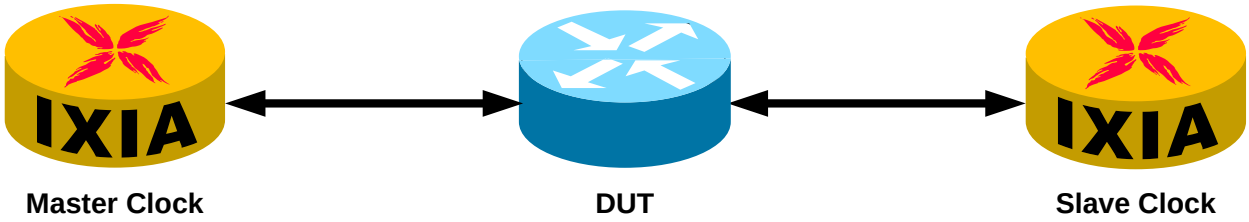


Figure 51. Correction Factor Error test setup

About Calibration

In order to measure the Correction Factor accurately, it is important to ensure that the IxN2X latency measurement is as accurate as possible, and that the timestamp plane is referenced to actual ingress and egress points of the messages to/from the DUT.

This will help eliminate inaccuracies that may otherwise be caused by:

- Internal offsets within IxN2X (between the point of insertion of timestamps and the test interface connector).
- The propagation delays within the cables connecting the DUT interfaces to the IxN2X test interfaces. For example, Category 5E electrical cable adds a propagation delay of **5.48 ns/m**, while optical fiber adds a delay of approximately **3.29 ns/m**.

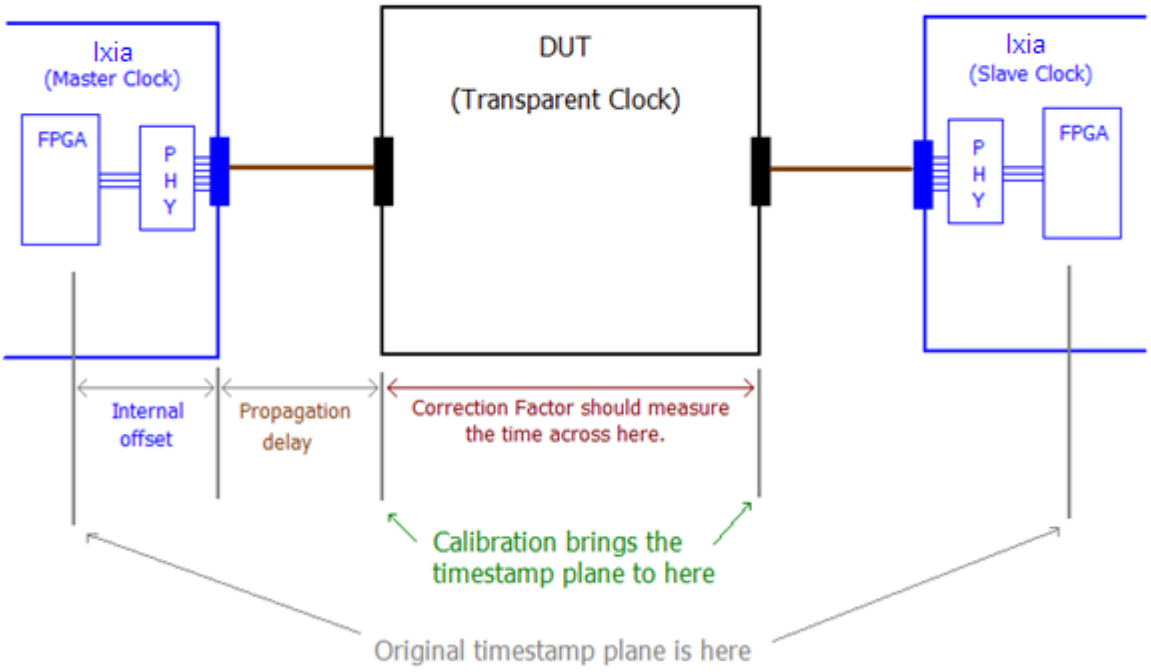


Figure 52. **Calibration helps correct for IxN2X offsets and cable propagation delays**

While the IxN2X already has some compensation for internal offsets built into its timestamp engine, it is not able to fully compensate for all aspects of the offsets and cannot automatically take propagation delay into account.

Configurations

There are two configurations for this test:

- **Calibration mode** configuration, for the calibration step, for which we will interconnect two IxN2X test ports back-to-back using **one Ethernet calibration cable**.
- **Test mode** configuration, for the measurement steps, for which we will connect two IxN2X test ports to two DUT test ports using **two Ethernet test cables** of **equal length**.

The length of the calibration cable must be equal to twice the length of one test cable. This is important and will help ensure that there is no contribution to the reported Correction Factor error caused by differing cable lengths.

In summary, you will need a total of **three cables** for this test:

- Two test cables of the same length (**x meters**) to connect the Master test interface to the DUT and to connect the DUT to the Slave test interface during the measurement steps. Measure the length of this cable.
- A calibration cable that is twice as long (**2x meters**) to connect the Master test interface directly to the Slave test interface during the calibration step.

Calibration mode

- The DUT is not required.
- Configure IxN2X with two test ports:
  - One test port will be used as Master port (on which we will emulate a Master Clock).
  - One test port will be used as a Slave port (on which we will emulate a Slave Clock).
- Connect the IxN2X Slave port to the IxN2X Master port using the **Ethernet calibration cable**.

Test mode

- Configure the DUT as a Transparent Clock with two ports:
  - One Slave port (to connect to the IxN2X Master port).
  - One Master port (to connect to the IxN2X slave port).
- Configure IxN2X with two test ports:
  - One test port will be used as Master port (on which we will emulate a Master Clock). Connect the IxN2X Master port to the DUT Slave port using **one of the Ethernet test cables**.
  - One test port will be used as a Slave port (on which we will emulate a Slave Clock). Connect the IxN2X Slave port to the DUT Master port using **the other Ethernet test cable**.

Step-by-Step Instructions

1. Calibrate the timestamps.

   If a calibration cable of the correct length cannot be obtained or constructed, you must still carry out the calibration procedure in order to account for the internal test equipment residual latencies. You may then use the above cable propagation-delay estimates to either determine or correct for the calibration error that is likely to result from using a calibration cable of incorrect length.

   a. Using the calibration cable, run the following steps (steps 2-7) using the default **zero** Tx and Rx Calibration factors for the Master and Slave emulations.
   b. Note the average **Sync Latency** and average **Delay Request Latency** measurements recorded after a period of time, once these measurements have settled.

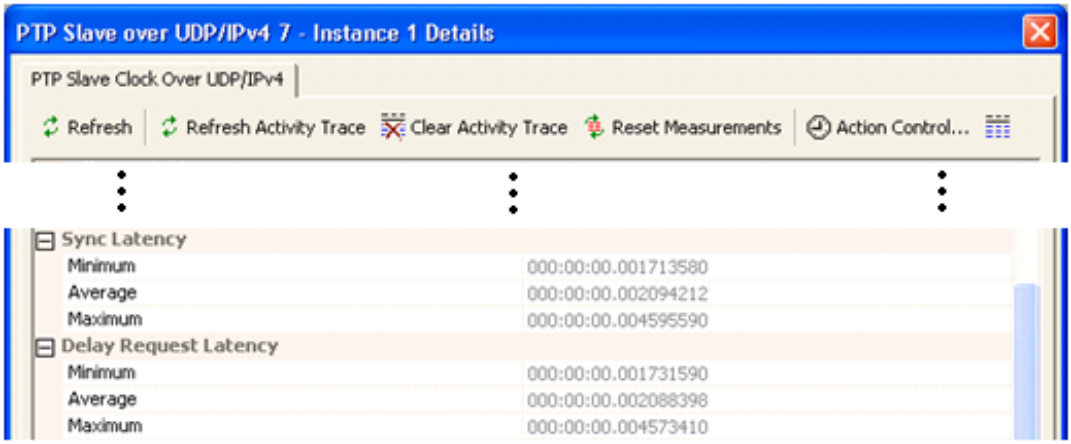


Figure 53. **Viewing the Sync Latency and Delay Request Latency Measurements**

c. Configure the **Master port** Tx and Rx calibration factors according to the following formulae:
   i. **Tx calibration factor** = Sync Latency / 2
   ii. **Rx calibration factor** = Delay Request Latency / 2

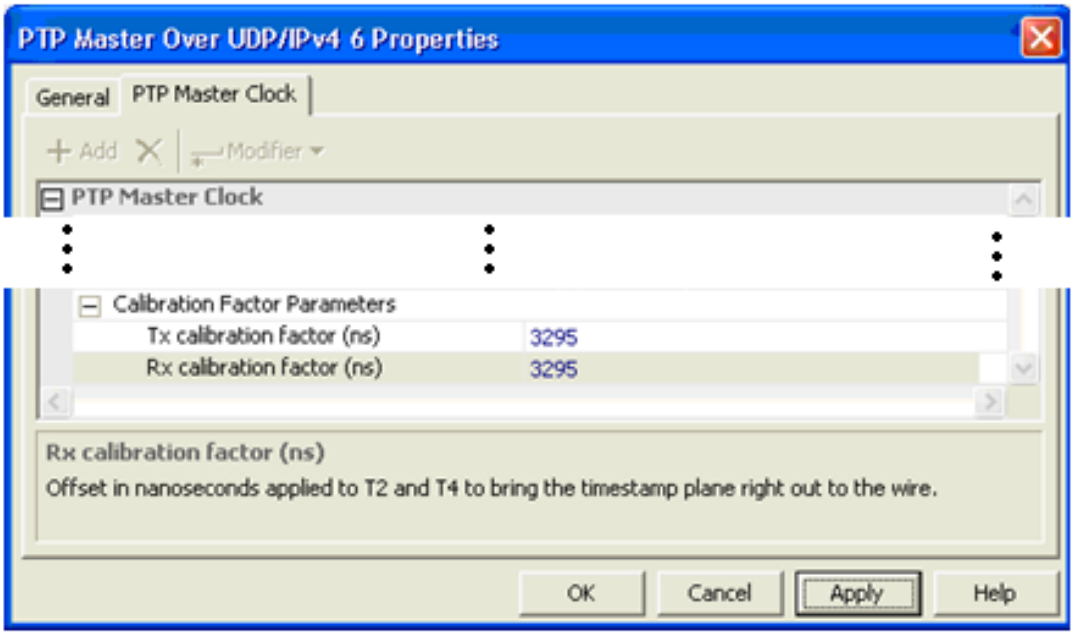


Figure 54. **Configuring the Master Clock Calibration Factors**

d. Similarly, configure the **Slave port** Tx and Rx calibration factors according to the following formulae:
   i. **Tx calibration factor** = Delay Request Latency / 2
   ii. **Rx calibration factor** = Sync Latency / 2

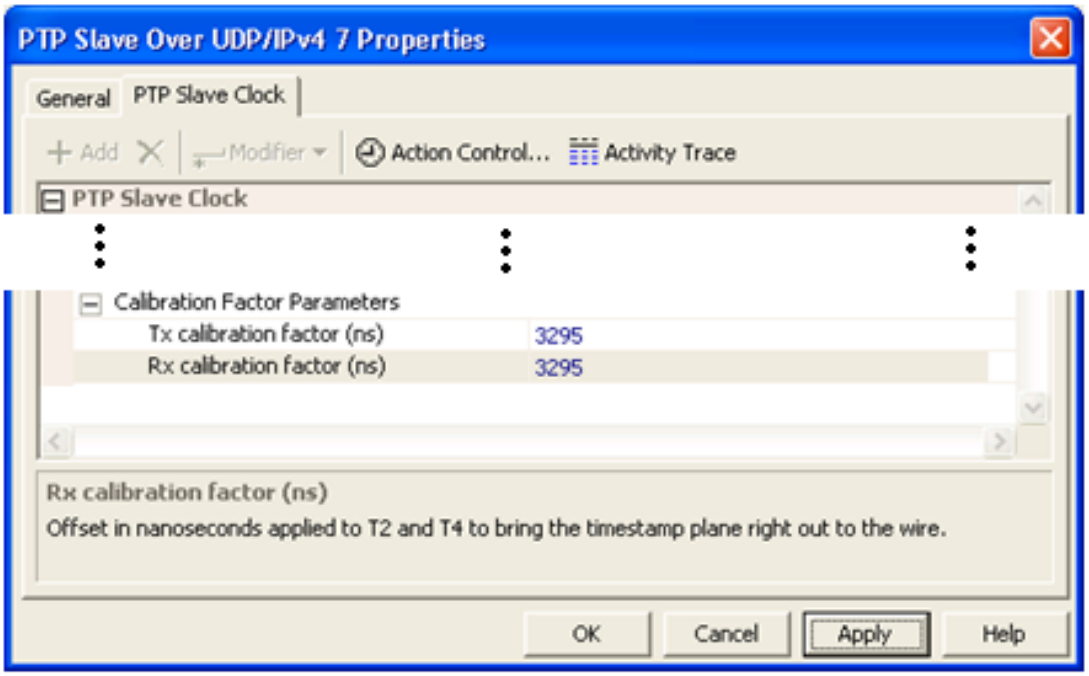


Figure 55. **Configuring the Slave Clock Calibration Factors**

2. Press the **Reset measurements** button within the Slave Results dialog. In the **Slave Details** dialog, check that:

   i. the **Sync Latency** is now close to zero (under 100ns).
   ii. the **Delay Request Latency** is now close to zero (under 100ns).
   iii. the **Latency Asymmetry** is now close to zero (under 50ns).
   iv. the **Offset From Master** (OFM) is now close to zero (under 100ns).

   It may be necessary to adjust the calibration factors slightly in order to zero out the latency values. To do so: Change the calibration values, press **Apply**, **Reset measurements** on the Slave, and then **Refresh** the Slave instance measurements to see the new latency values.

   Note that the magnitudes of the residual latencies and the stability of the calibrated values will vary according to the type of IxN2X test card used and the line rate (10/100/1000/10000 Mb/s) used.

   Once IxN2X is properly calibrated, the measured **Sync Latency** and **Delay Request Latency** values will accurately represent the actual PTP packet residence time in the DUT, excluding some small residual internal IxN2X offsets (e.g., variable PHY delays) and propagation delays in the cables. Note that the IxN2X real-time **traffic-based Latency** measurements remain unchanged and will be larger than the **PTP emulation Latency** measurements.

3. Configure the link layer and IP addresses on the IxN2X Master port (the port that will emulate the Master Clock) and on the IxN2X Slave port (the port that will emulate the

Slave Clocks). Assuming that the Transparent Clock DUT is an Ethernet switch, which is transparent to layer 3:

a. Configure the **First Address** of the Slave port (shown as port 101/1 below) to 192.1.1.2.
b. Configure the **First Address** of the Master port (shown as port 101/2 below) to 192.1.1.1.
c. Configure the Slave port's **SUT Interface** IP address to 192.1.1.1/24 (i.e., to match the Master port).
d. Configure the Master port's **SUT Interface** IP address to 192.1.1.2/24 (i.e., to match the Slave port)
e. Press the **Send All ARP Requests** button.

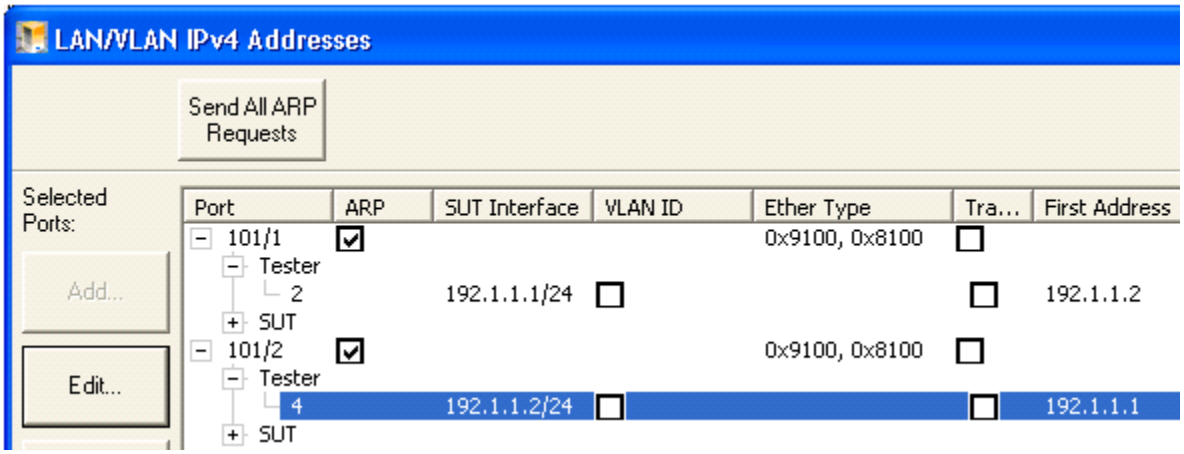


Figure 56. **Configuring the IP Addresses of the DUT and IxN2X Test Ports and DUT**

4. Create one Master Clock emulation on the Master port (101/2).

   a. Use the default configuration parameters.
   b. Change the Sync message rate to 8 packets per second.

5. Create one Slave Clock emulation on the Slave port (101/1).

   a. Within the Slave Clock Properties dialog box, in the PTP Slave Clock tab, uncheck **Apply random distribution**. This ensures that the emulation will not transmit a request before a response has been received to the previous request.

b. Set the **Log Minimum Delay Request Interval** to 0 (1 message per second).

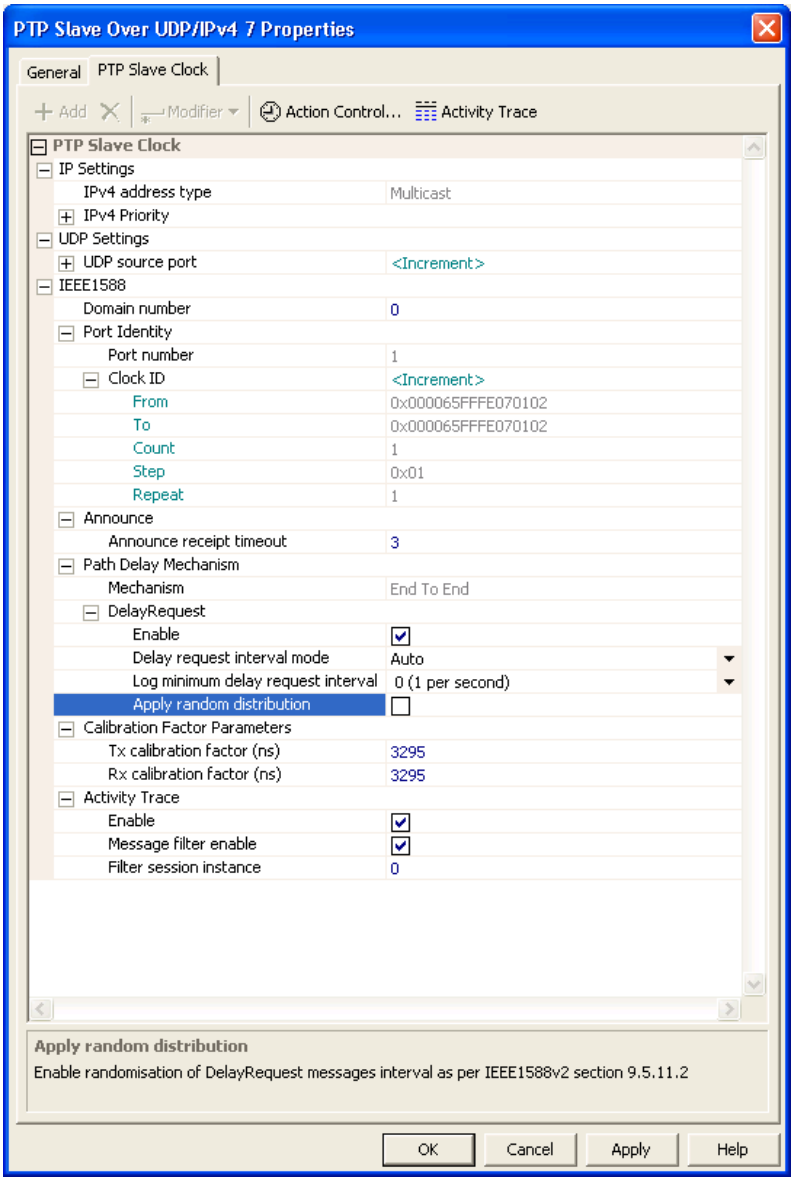


Figure 57. **Configuring the PTP Slave Clock Emulation**

6. Enable the devices (Master and Slave) by checking the device emulation checkboxes on the main window.

7. Wait for the Slave device to transition to the **Slave** state.

8. Measure Correction Factor Error

   a. In the **Setup – Emulation** area, select the **PTP Slave** emulation.
   b. Click the **Details** button. The PTP Slave Instances dialog box is displayed.
   c. Double-click the table row that reflects the Slave instance.

d. Scroll down the Slave Instance Details window to view the Slave's **Sync Correction Factor Error** and **Delay Request Correction Factor Error** measurements:
   i. Minimum
   ii. Average
   iii. Maximum

e. Use the **Refresh** or **Reset Measurements** buttons to control your view of the statistics.

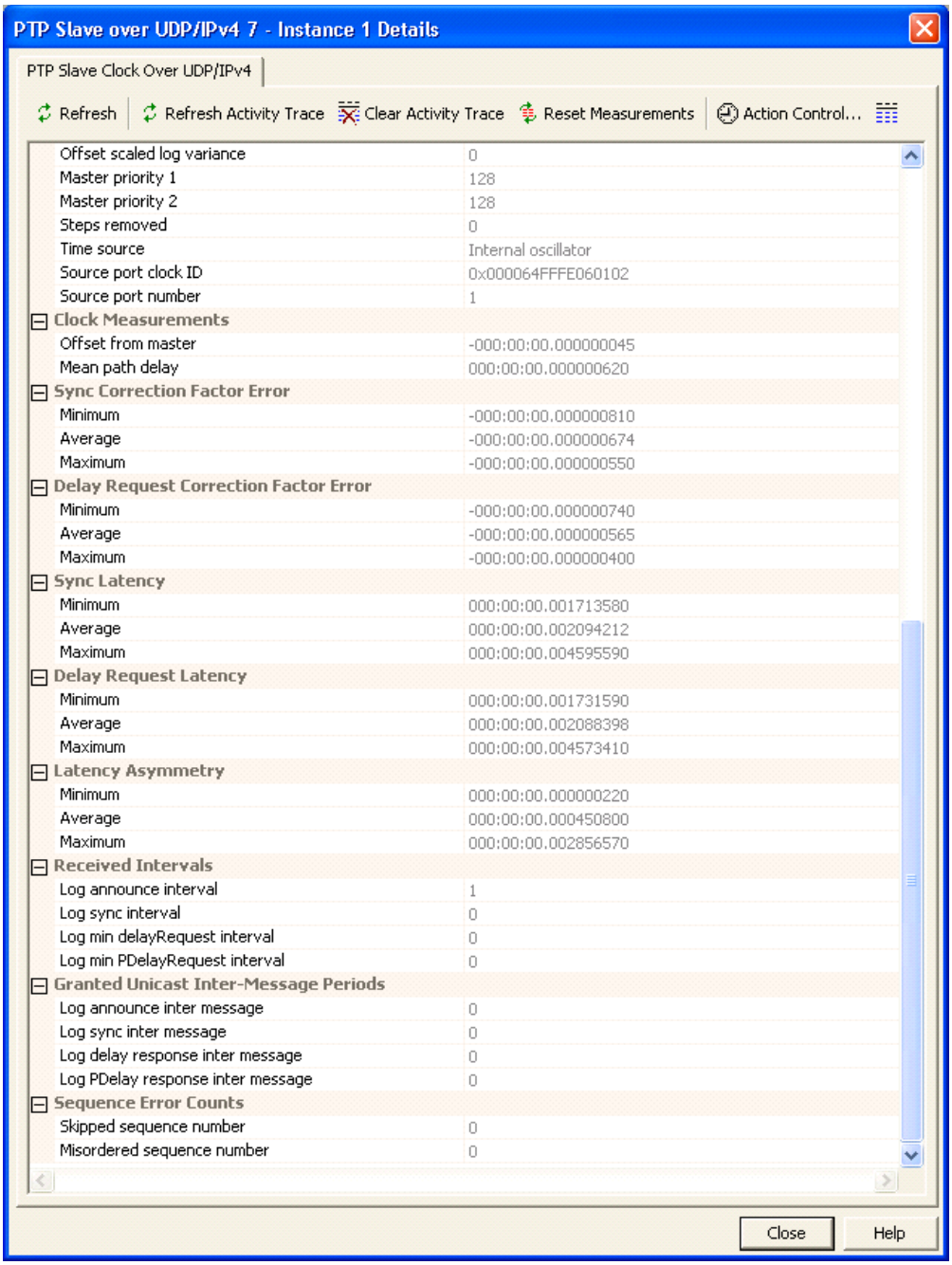


Figure 58. **Measuring the Correction Factor Errors**

Test Variables

Repeat the test with the following suggested variations:

- Increase the Sync and Delay Request **message rates** as required.
- Increase the **number of slaves** emulated on the slave port to 100, depending on the expected load in the target system. (See also PTP 02 Slave Scalability).
- Run the test across **different pairs of ports**, across port pairs in **both directions** at the same time (using different clock domains), and across **multiple port pairs** at the same time. This is advisable because port asymmetries and unexpected performance differences have been found in at least one commercial Transparent Clock, and because testing on multiple port pairs at the same time may load the DUT and impact the Correction Factor accuracy.
- Run the test on **multiple clock domains** simultaneously. This will test whether the Transparent Clock DUT is able to be syntonized to multiple upstream Master Clocks (on different clock domains) at the same time. A lack of syntonization of the Transparent Clock will cause its time base (for CF calculations) to be inaccurate. This may cause a CF Error result that is higher than expected and increases linearly with increasing forwarding latency.
- Introduce **background data-plane (user) traffic** by creating non-PTP traffic streams to and from the Master and Slave ports.
- Add a **control-plane load**, for example by emulating the Spanning Tree Protocol (STP) or other protocols, and rapidly changing the protocol parameters or flapping the emulated devices.
- Run the test in both PTP **multicast** mode and PTP **unicast** mode.

Results Analysis

The measured Correction Factor Error should be less than the DUT specification or less than the requirements of the target system or network, under all conditions that might be expected. Generally, the Correction Factor error should be less than a few hundred nanoseconds; however, this varies depending on the application of your DUT.

Conclusions

Correction Factor Error contributes to the time offset experience by each Slave Clock in a system.

The application's timing synchronization requirements will determine the maximum time offset permitted at each Slave Clock. If Transparent Clocks are used in the system, then some of this maximum time offset must be budgeted or allocated to Correction Factor Error. However, **multiple** Transparent Clocks are likely to be used in a real network, so the permitted Correction Factor Error of any single Transparent Clock must be **reduced** according to the maximum number of TCs expected to be **cascaded**.

Test Case: ESMC Best Reference Port Selection by Using IxNetwork

Overview

ESMC uses the Synchronization Status Messages (SSM) PDU, which runs directly over Ethernet. The SSM PDU is essentially a 'heartbeat' message, which provides a continuous indication of the clock quality level. The default message period is usually one per second that is within the requirements of the IEEE 802.3 Slow Protocols, which cannot exceed 10 per second. To minimize the effects of wander that may occur during holdover, an Event type message with a new SSM quality level is generated immediately. The SSM code contained in the Quality Level (QL) TLV represents the free-run accuracy of the clock that is currently the clock source of the synchronization trail.

As a reference, Network Level SSM is defined in the G.781 specification.

IEEE assigned OUI and Slow protocol subtype

Organizational Specific Identifier	**0x0019A7**
Slow Protocol Subtype	0X0A

ESMC PDU format

Octet number	Size	Field
1-6	6 octets	Destination Address =01-80-C2-00-00-02 (hex)
7-12	6 octets	Source Address
13-14	2 octets	Slow Protocol Ethertype = 88-09 (hex)
15	1 octets	Slow Protocol Subtype =0A (hex)
16-18	3 octets	ITU-OUI = 00-19-A7 (hex)
19-20	2 octets	ITU Subtype
21	4 bits	Version
	1 bit	Event flag
	3 bits	Reserved
22-24	3 octets	Reserved

Octet number	Size	Field
25-1532	36-1490 octets	Data and Padding (See point J)
Last 4	4 octets	FCS

QL TLV format

8 bits	Type: 0x01
16 bits	Length: 0x04
4 bits	0 (unused)
4 bits	SSM code

SSM Quality Level Codes

SSM QL Code			QL Code interpretation for Synchronous Ethernet G.8274, and each G.781 Synchronization Philosophy				Ixia Label for decodes/encodes
Dec	Bin	Hex	G.8274	Option I	Option II	Option III	
0	0000	00	-	QL-INV0	QL-STU	QL-UNK	QL-STU/UNK
1	0001	01	-	QL-INV1	QL-PRS	QL-INV1	QL-PRS
2	0010	02	-	QL-PRC	QL-INV2	QL-INV2	QL-PRC
3	0011	03	-	QL-INV3	QL-INV3	QL-INV3	QL-INV3
4	0100	04	-	QL-SSU-A	QL-TNC	QL-INV4	QL-SSU-A/TNC
5	0101	05	-	QL-INV5	QL-INV5	QL-INV5	QL-INV5
6	0110	06	-	QL-INV6	QL-INV6	QL-INV6	QL-INV6
7	0111	07	-	QL-INV7	QL-ST2	QL-INV7	QL-ST2
8	1000	08	-	QL-SSU-B	QL-INV8	QL-INV8	QL-SSU-B
9	1001	09	-	QL-INV9	QL-INV9	QL-INV9	QL-INV9
10	1010	0A	QL-EEC2	QL-INV10	QL-ST3	QL-INV10	QL-EEC2/ST3
11	1011	0B	QL-EEC1	QL-SEC	QL-INV11	QL-SEC	QL-EEC1/SEC

SSM QL Code			QL Code interpretation for Synchronous Ethernet G.8274, and each G.781 Synchronization Philosophy				Ixia Label for decodes/encodes
12	1100	0C	-	QL-INV12	QL-SMC	QL-INV12	QL-SMC
13	1101	0D	-	QL-INV13	QL-ST3E	QL-INV13	QL-ST3E
14	1110	0E	-	QL-INV14	QL-PROV	QL-INV14	QL-PROV
15	1111	0F	-	QL-DNU	QL-DUS	QL-INV15	QL-DNU/DUS

Objective

The purpose of this use case is to verify that the DUT correctly selects the source reference port with the best reported Quality Level (QL).

The SSM code contained in the QL TLV represents the free-run accuracy of the clock that is currently the clock source of the synchronization trail. Specific bounds on the processing times of messages are defined in G.781.

When a network element is operating in the QL enabled mode, the protocol generation and reception must meet the criteria below in ITU-T G.8264 section 11.3.2.1 and 11.3.2.2 respectively. The synchronization selection function in Annex A of G.781 has been modeled by using SDL descriptors. The critical aspects of the algorithm are based on the input quality level of each of p inputs (that is, QL[p] in G.781). The output QL, QL_out, is the SSM code that is to be transmitted on output ports of the NE. G.781 describes cases where DNU is applied instead of the active quality level. Note that Annex A of G.781 is normative; it describes the network equipment behavior. It does not necessarily mandate a specific implementation.

Synchronization Status Messages are required to allow the downstream element that requires synchronization to know the quality of the upstream clock.

The synchronization message shall be ’pushed’ from device to device that supports synchronous Ethernet. At each device that supports Synchronous Ethernet, the message shall be processed and acted on. The message set shall then be remade and passed to the next downstream element.

To test this algorithm, the three test ports connected to the DUT will be configured to be one of a high value, one of a low value, and one to Do Not Use as follows:

- Test Port 1: QL-PRS (Primary Reference Source)
- Test Port 2: QL-DNU/DUS (Do Not Use, lowest option)
- Test Port 3: QL-ST2 (lower level than PRS)

The expected behavior is for the DUT to select the reference port connected to Test Port 1 advertising QL-PRS.

NOTE: It is important to know how the DUT ESMC algorithm has been implemented and select the appropriate QL as found in the SSM Quality Level Codes table.

Setup

The following figure demonstrates the physical setup of the test bed:

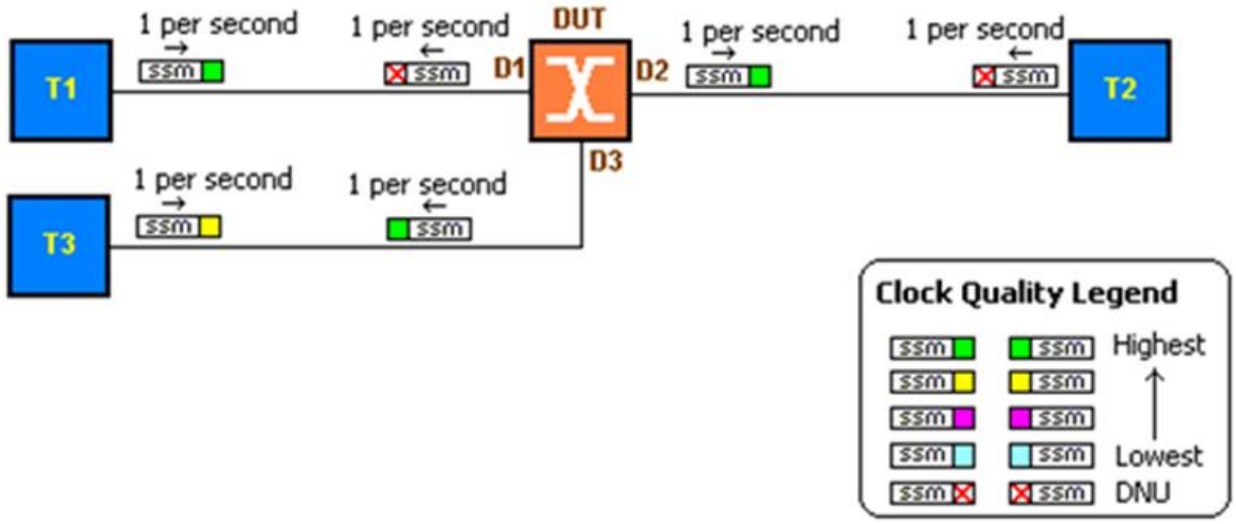


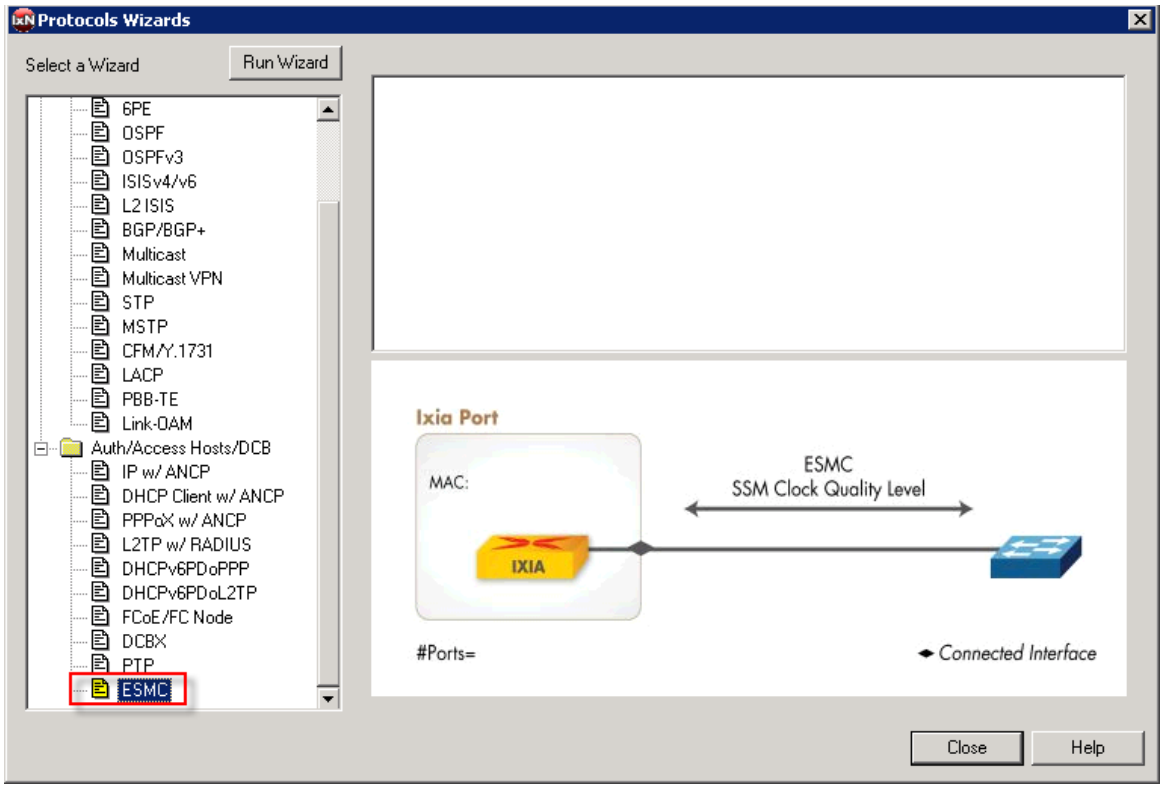
Figure 59. Test topology and SSM PDU exchange

Step-by-Step Instructions

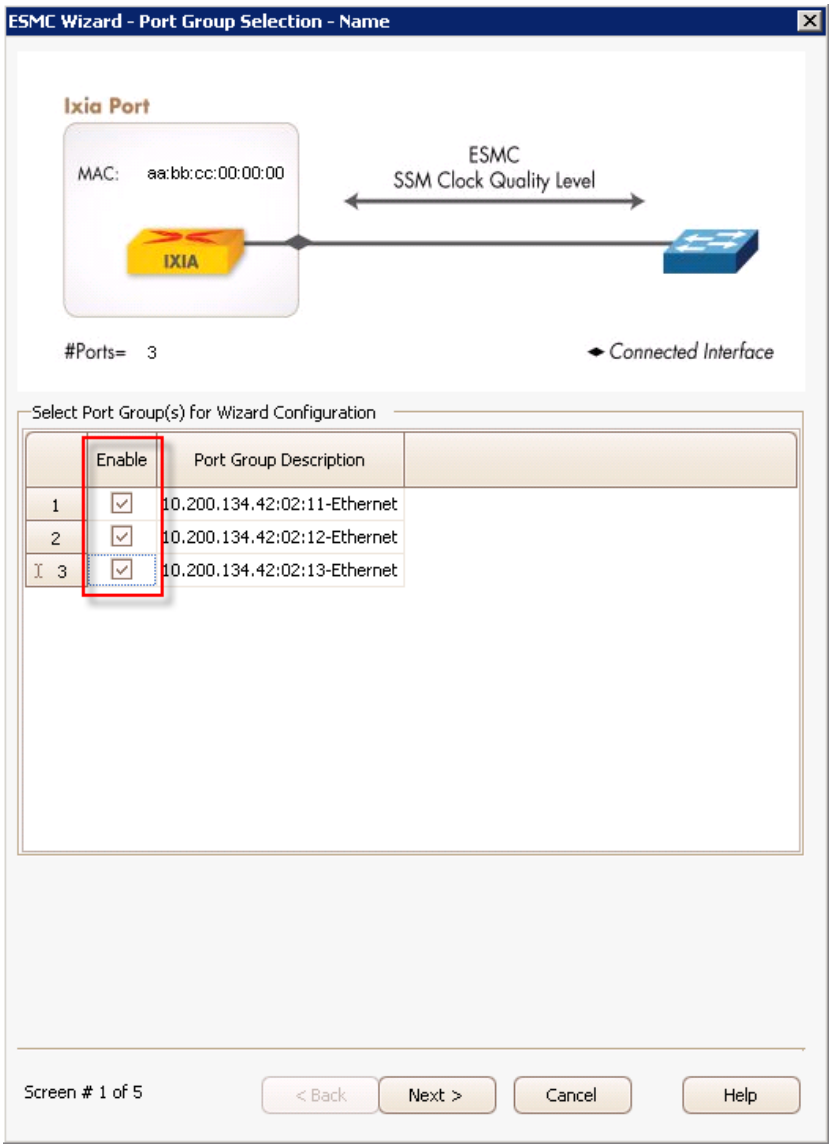
Use the following procedure for this test case:

1. After connecting to the Ixia chassis and reserving three ports, run the Protocol Wizard to Configure ESMC:

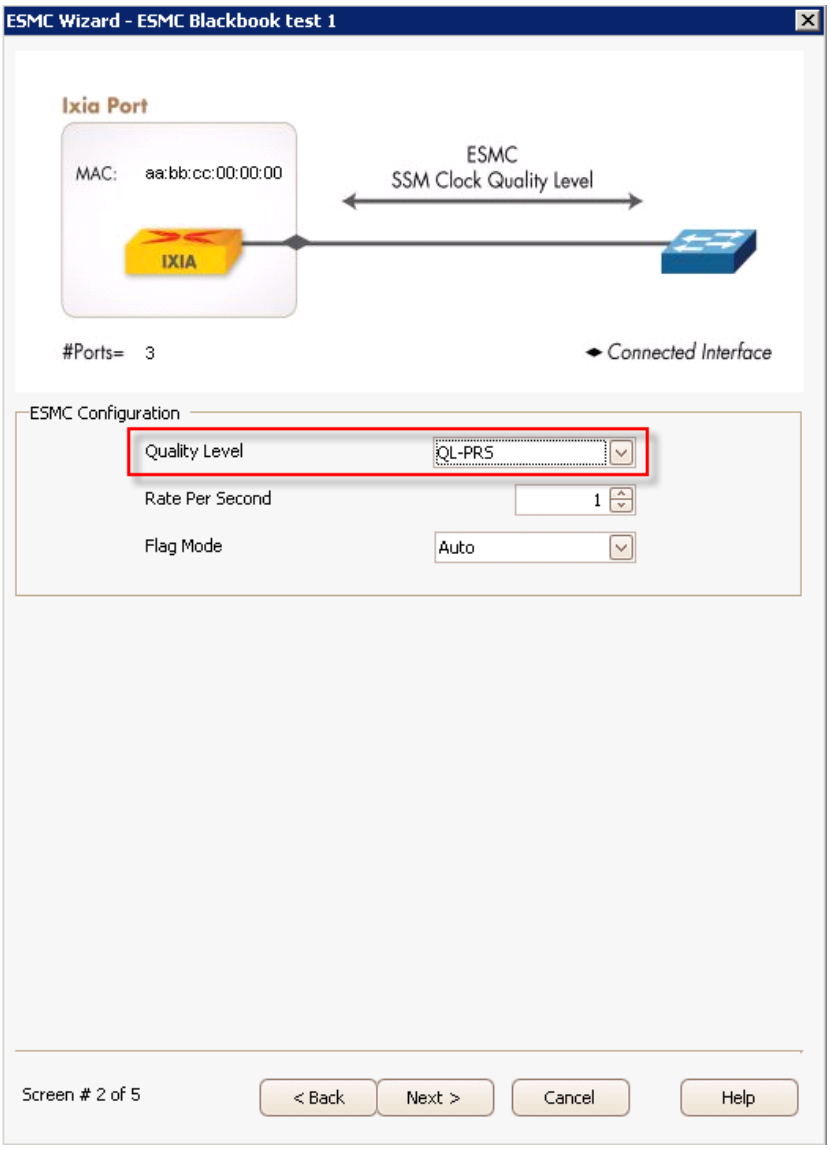
   a. Start the **Protocol Wizard** by using the button on the top toolbar**,** select **ESMC** under **Auth/Access Hosts** and click **Run Wizard**.



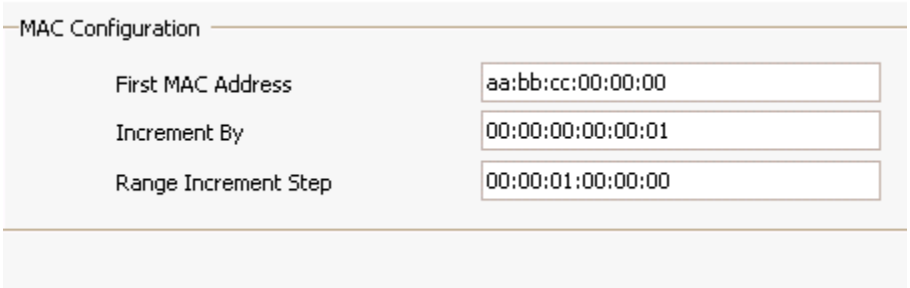
b. In the next screen, select the ports that you want to enable ESMC on.



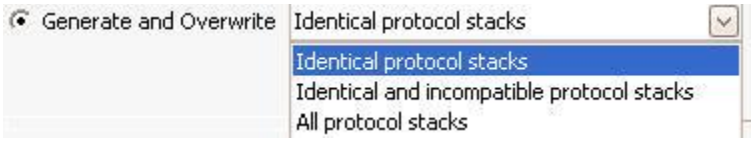
c. In the next screen, select the ESMC configuration options. Start with the Quality level of QL-PRS. PRS is Primary Reference Source, which is one of the highest Quality Level options.



d. In the next screen, configure the MAC address information.

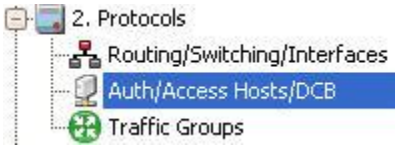


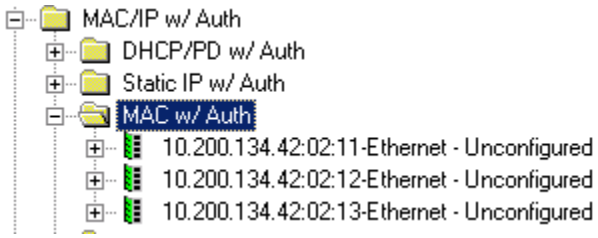
e. The next screen is dedicated for (optional) VLAN Configuration. Note: VLAN is not typically configured with ESMC.
f. In the next screen, select the name of the configuration, click **Generate and Overwrite** select **All protocol stacks**, and then click **Finish** to complete the protocol wizard.

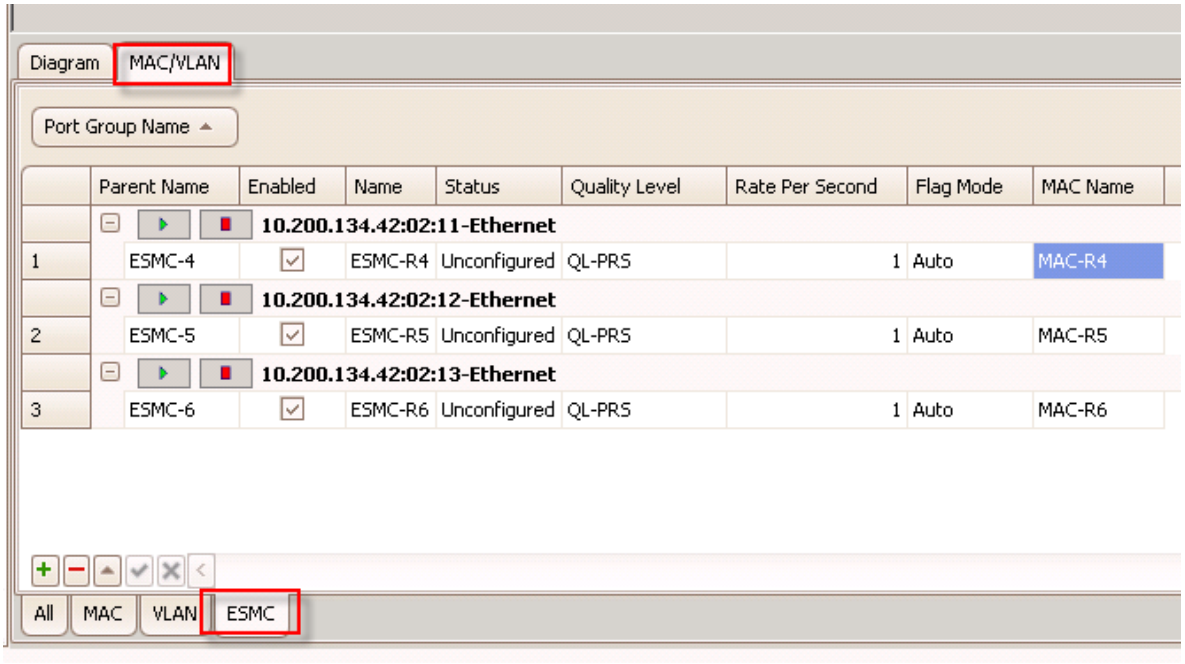


Tip: Name this configuration profile for the wizard and it will be available in the list the next time this wizard is selected. Double click the name to open the configuration profile in the wizard.

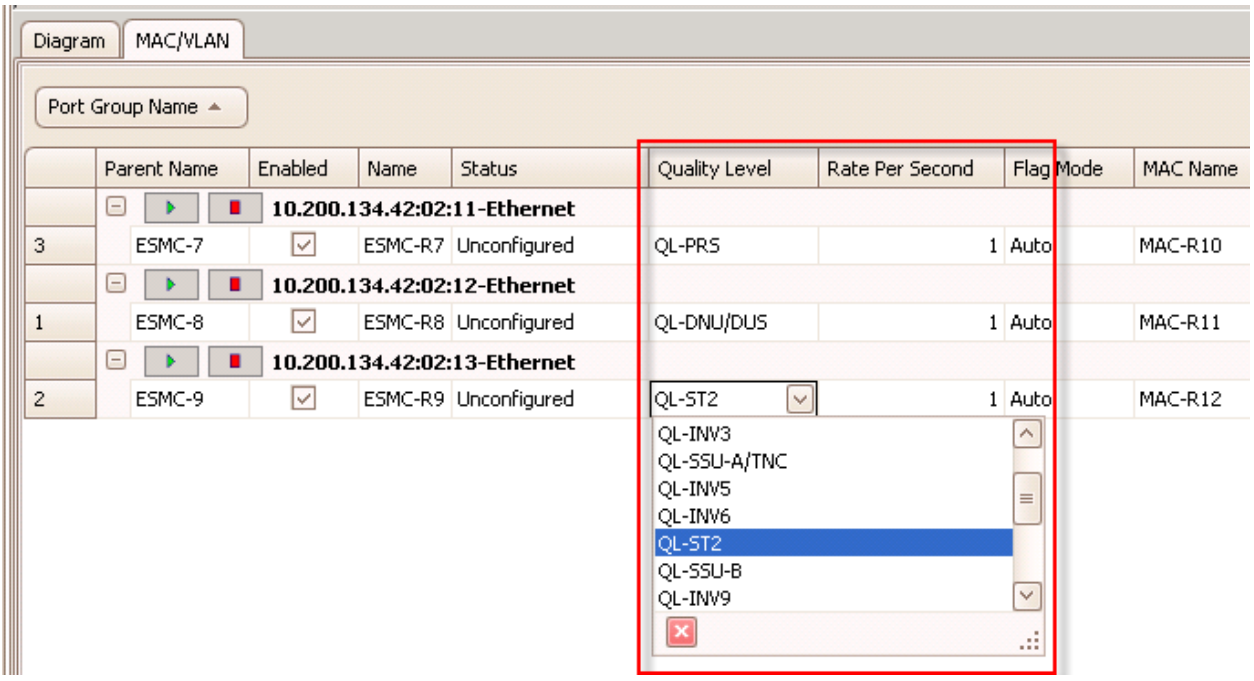
g. Click **Close** on the Protocol Wizards screen. Click **Auth/Access Hosts/DCB** in the Test Configuration list. Next, select the **MAC/IP w/Auth** folder. ESMC will be the enabled ports under the **MAC w/Auth** folder. Click the **MAC/VLAN** tab on the upper right, and then the lower **ESMC** tab will show the ESMC configuration.



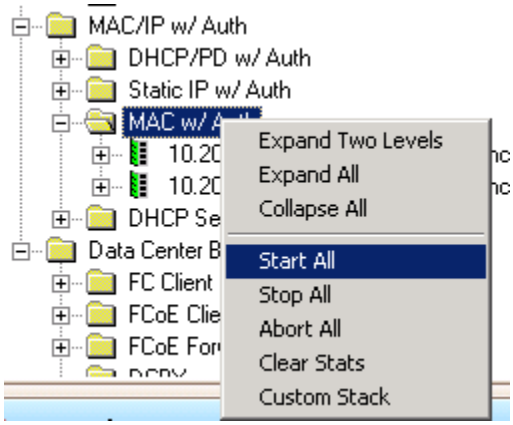




2. Configure the Quality Level as follows:
   a) Test Port 1: QL-PRS (Primary Reference Source)
   b) Test Port 2: QL-DNU/DUS (Do Not Use, lowest option)
   c) Test Port 3: QL-ST2 (lower level than PRS)

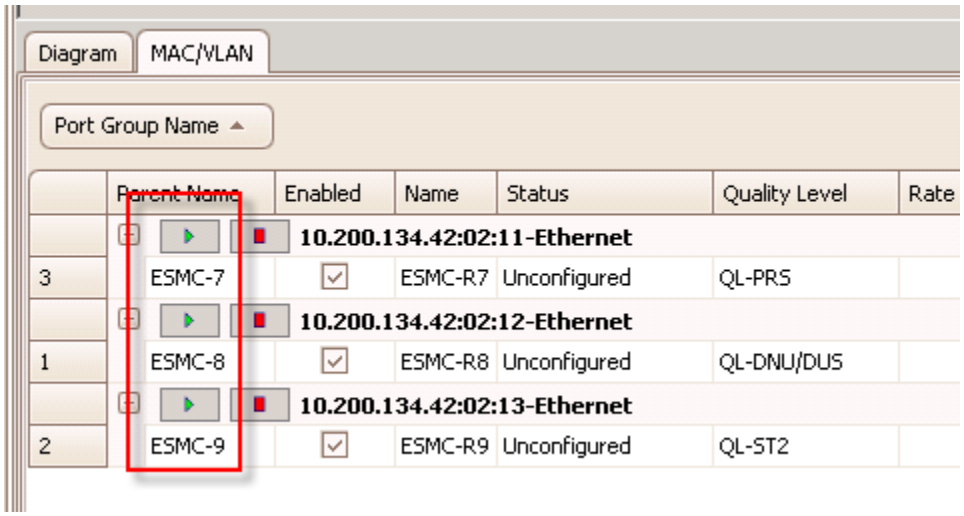


3. Start the Protocol.
   Right-click the folder and select **Start All.** This will start the protocols configured by using the ESMC wizard.



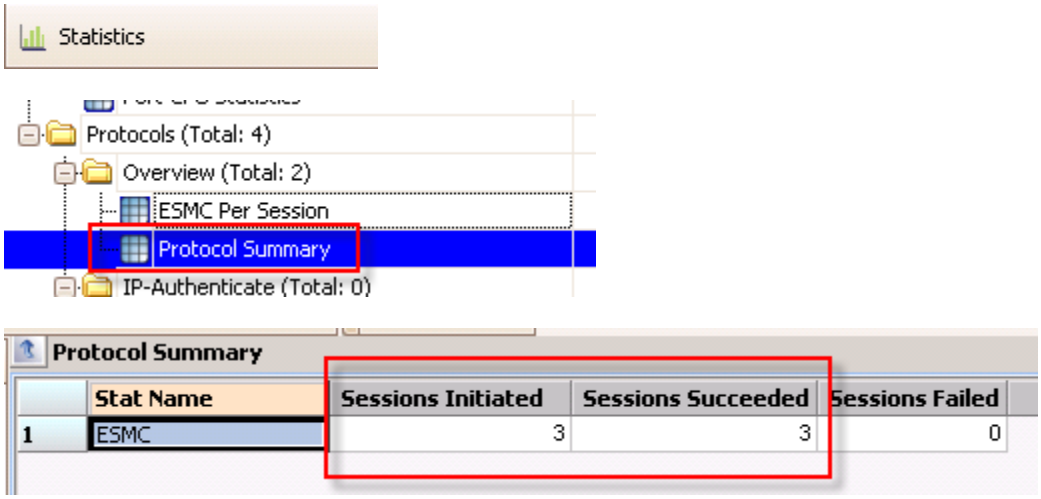
Tip: Click **Start All Protocols** on the top toolbar to start ALL protocols configured at the same time.

Tip: ESMC can be started by using the play buttons in the configuration grid.



Once up and running successfully, the Status should be 'Transmitting' on the **ESMC** bottom navigation tab.

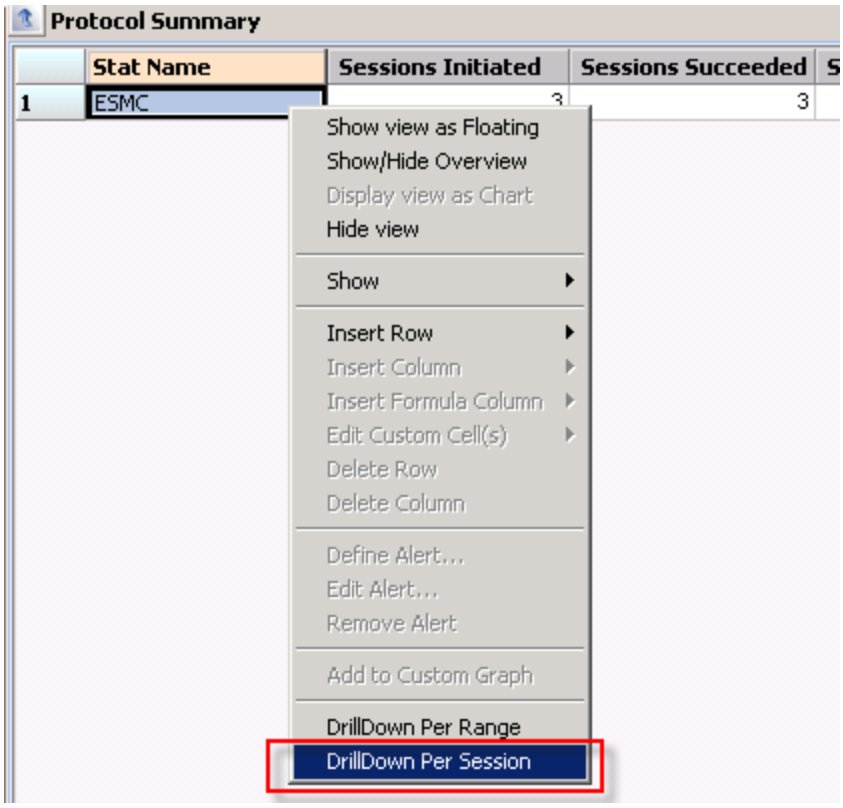
4. Verify the Protocol by using the Statistics Viewer.
   Click **Statistics** in the GUI navigation, and then select the **Protocol Summary** view under **Protocols** to verify that the sessions are successful.

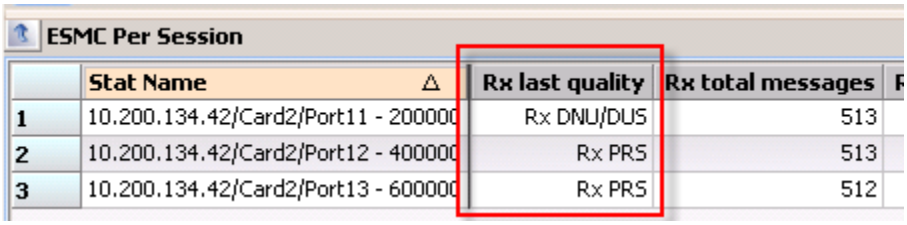


Results Analysis

The DUT should do the following:

- Recognize that QL received on D1 (QL-PRS) is the highest quality reference that it can see (verify on the DUT).
- Select the port from T1 as its reference port and physically switch to use the recovered clock from that port to drive its internal clock and hence, all output line clocks (verify on the DUT).
- Change to advertising QL-PRS quality to all downstream ports except the port that it is receiving QL-PRS on, which should be sending QL-DNU/DUS (verify in IxNetwork StatViewer).





Conclusions

Using the IxNetwork ESMC emulation, you can send SSM PDUs with different Quality Levels on each port and ensure that the DUT selects the best reference port QL, and then advertises it to downstream ports. It is also important to verify that it transmits QL-DNU/DUS to the port that it is receiving the best Quality Level from.

The Best Reference Port Selection process is described in G.8264/Y.1364 section 11.3.2.

Test Case: ESMC Port Switching by Using IxNetwork

Objective

The purpose of this use case is to verify that the DUT correctly switches its reference port selection when the best reported Quality Level (QL) has changed.

This test simulates an upstream clock change because of a network reconfiguration, outage, or recovery. It could also be because of an upstream device switching its clock source (for example, because of a GPS failure).

To test this algorithm, the three test ports connected to the DUT will be configured to be one of a high value, one of a low value, and one to Do Not Use as follows:

- Test Port 1: QL-PRS *Changed* to QL-ST2
- Test Port 2: QL-DNU/DUS (Do Not Use, lowest option)
- Test Port 3: QL-ST2 *Changed* to QL-PRS

The expected behavior is for the DUT to change the selected reference port connected from Test Port 1 to Test Port 3 advertising QL-PRS.

Note: It is important to know how the DUT ESMC algorithm has been implemented and select the appropriate QL as found in the SSM Quality Level Codes table.

Reference standard ITU-T 11.3.2 and Annex A.

Setup

The following figure demonstrates the physical setup of the test bed:

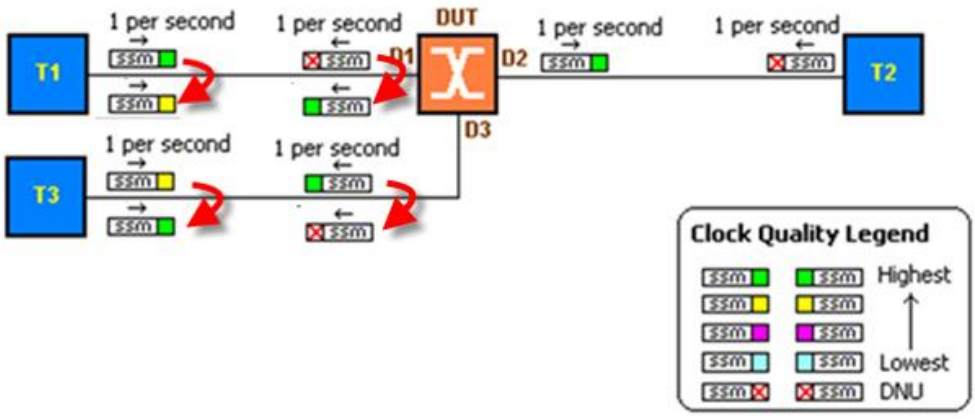
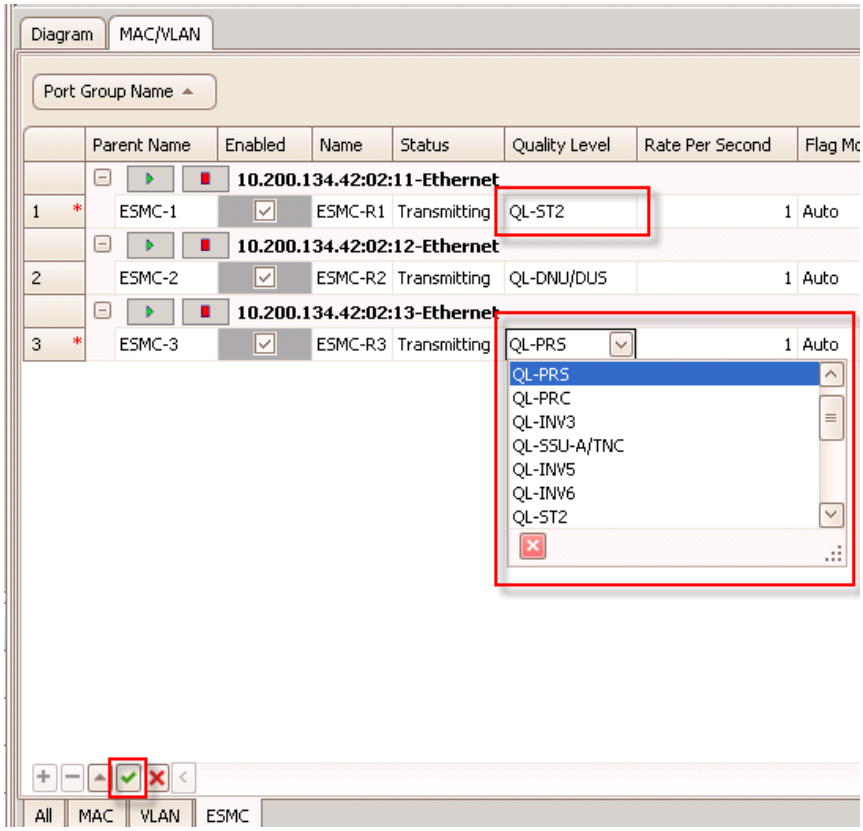


Figure 60. Test topology and SSM PDU exchange with the QL changed on Test Ports 1 and Test Ports 3

Step-by-Step Instructions

Use the following procedure for this test case:

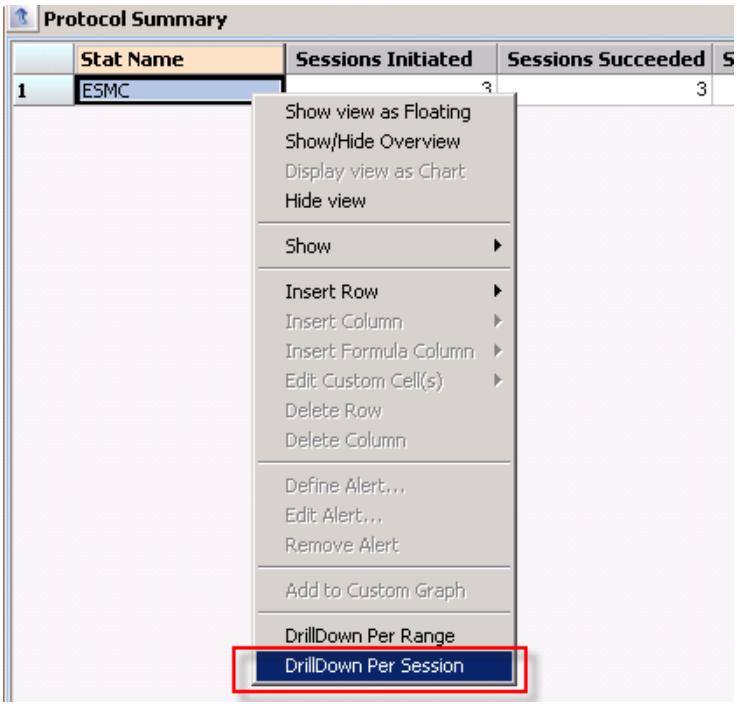
1. Starting with the running configuration from ESMC Test 1, on the ESMC tab of the configuration, change the Quality Level of Test Port 1 to QL-ST2 and the Quality Level of Test Port 3 to QL-PRS. Click the green check icon to commit the changes. (This change will be applied on the fly without requiring a stop/start of the running protocol.)

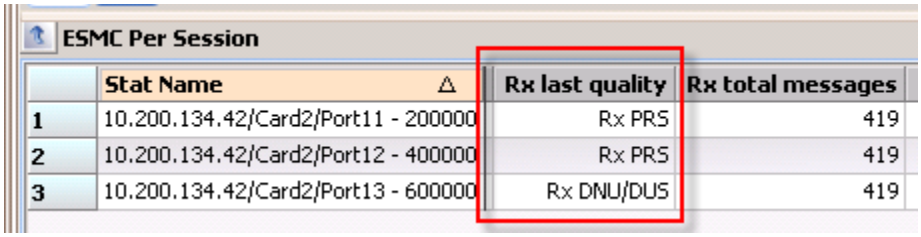


Results Analysis

The DUT should do the following:

- Recognize that QL received on D3 (QL-PRS) is now the highest quality reference that it can see (verify on the DUT).
- Select the port from T3 as its reference port and physically switch to use the recovered clock from that port to drive its internal clock and hence, all output line clocks (verify on the DUT).
- Change to advertising QL-PRS quality to all downstream ports except the port that it is receiving QL-PRS on, which should be sending QL-DNU/DUS (verify in IxNetwork StatViewer).





Conclusions

IxNetwork ESMC emulation can be configured to send SSM PDUs with different Quality Levels on each port and ensure that the DUT selects the best reference port QL, and then advertises it to downstream ports. As a secondary test, the Quality Level can be changed, simulating a network change, and it can be validated that the DUT is able to switch selected reference ports. It is also important to verify that it transmits QL-DNU/DUS to the port that it is receiving the best Quality Level from.

The Best Reference Port Selection process is described in G.8264/Y.1364 section 11.3.2.

Test Case: ESMC Failover (5-Second Rule) by Using IxNetwork

Objective

The purpose of this use case is to verify that the DUT correctly implements the failover 5-second rule.

From the ITU-T Standard G.8264 section 11.3.2.2 QL Reception:

The QL state, QL_out is used by synchronization selection algorithm described in G.781(see G.781 Annex A). For Synchronous Ethernet, the slow protocol used for the transmission of the SSM code relies on the use of a 'heartbeat' timer. ESMC Information PDUs are sent periodically at a rate of one PDU per second. Lack of reception of an ESMC Information PDU within a five-second period results in the QL being set to DNU.

The default (initial) value for the QL is DNU and must only change when a valid QL TLV is received.

On reception of an Event TLV, the QL state is changed to the new QL value, and the information timer is reset.

If the NE is operating in QL enabled mode and no QL TLV is received within a five-second period, the QL state is set to DNU. The synchronization reference is now subject to a wait to restore period as defined in G.781.

This test simulates a failure where the primary reference port stops receiving ESMC PDUs and after five seconds will set it to DNU and switch to the next best reference clock port.

To test this algorithm, the three test ports connected to the DUT will be configured as follows:

- Test Port 1: QL-ST2
- Test Port 2: QL-DNU/DUS (Do Not Use, lowest option)
- Test Port 3: QL-PRS *Change rate of SSM to 0*

The expected behavior is for the DUT to change the selected reference port connected from Test Port 1 to Test Port 1 advertising QL-ST2 after the five second timeout.

Note: It is important to know how the DUT ESMC algorithm has been implemented and select the appropriate QL as found in the SSM Quality Level Codes table.

Reference standard ITU-T 11.3.2 and Annex A.

Setup

The following diagram demonstrates the physical setup of the test bed:

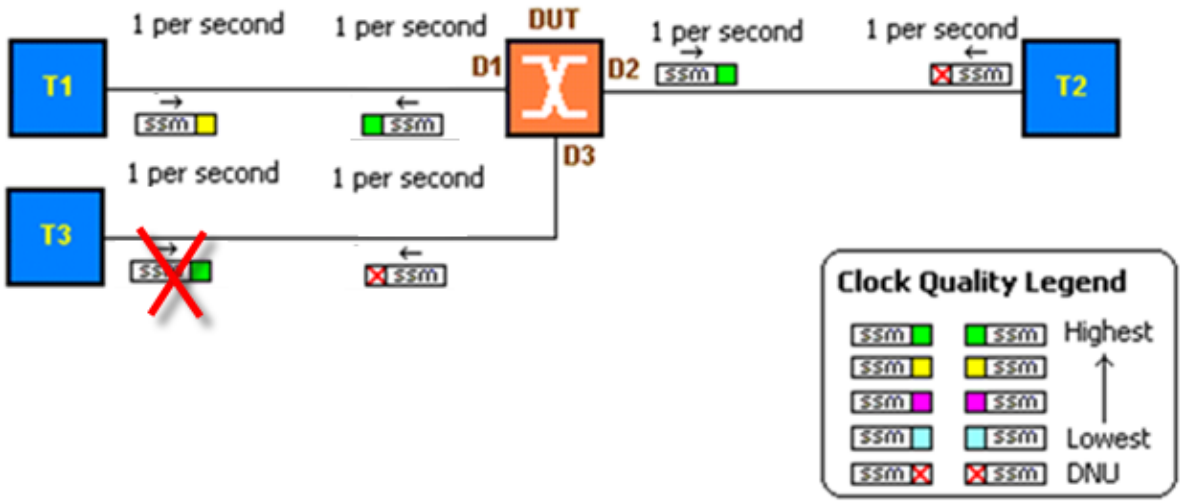
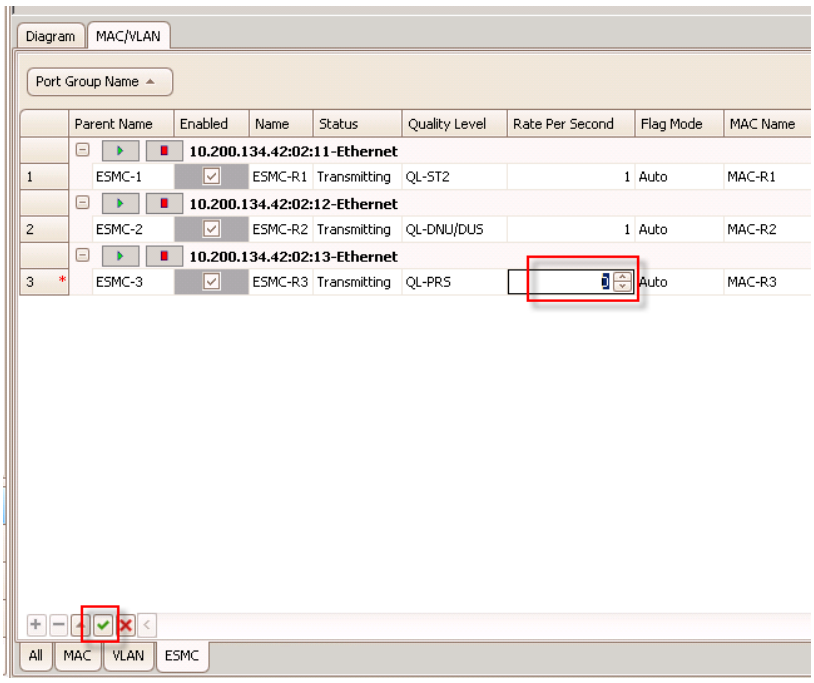


Figure 61. **Test topology and SSM PDU exchange and the rate of the SSM on Test Port 3 will be changed to 0**

Step-by-Step Instructions

Use the following procedure for this test case:

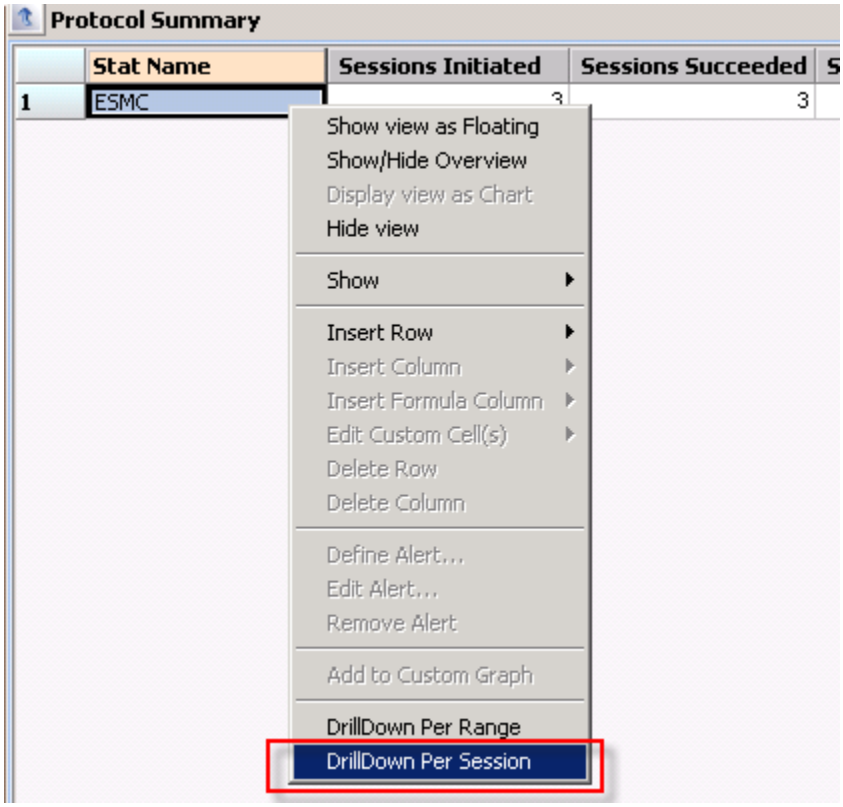
1. Starting with the running configuration from ESMC Test 2, on the ESMC tab of the configuration, change the Rate Per Second of the SSM on Test Port 3 from 1 to 0. Click the green check icon to commit the changes. (This change will be applied on the fly without requiring a stop/start of the running protocol).

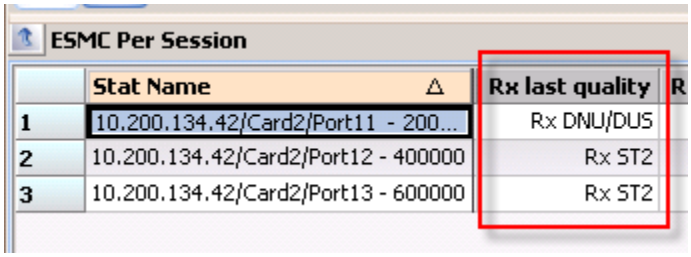


Results Analysis

The DUT should do the following:

- Recognize that it stopped receiving QL messages on D3 and after five seconds, switch over to the second best QL that is being received on D1(QL-ST2) (verify on the DUT).
- Change to advertising QL-ST2 quality to all downstream ports except the port that it is receiving QL-ST2 on, which should be sending QL-DNU/DUS (verify in IxNetwork StatViewer).





Conclusions

IxNetwork ESMC emulation can be configured to send SSM PDUs with different Quality Levels on each port and ensure that the DUT selects the best reference. It also has the ability to perform negative testing such as changing the SSM rate to 0 messages per second simulating a failure scenario. This provides the ability to test the failover (5-second rule) as defined in G.8264. After the five seconds, the DUT should select the best QL and advertise it to downstream ports.

ESMC Test Variables

Additional Test Cases

- SSM decode and analysis
- Validate SSM PDU generation
- Reference port flapping
- Slow Protocol interaction
- Negative test – SSM PDU
- Negative test – SSM flood
- SSM saturation
- SSM received PDU rate
- Egress QL matches configured QL
- Egress QL matches ingress QL
- Quality Level change propagation
- Multiport stress test
- Performance under load
- Clock synch and jitter (requires other testers)

Testing Ethernet Synchronization Clock Quality

Synchronization over Ethernet networks may carry synchronization data such as timestamps within the packets themselves, or they may use the Ethernet physical layer clock for synchronization directly. Emerging networks use a combination of both methods. Inaccuracy in the time and frequency synchronization may result from packet-layer impairments such as PDV, physical-layer impairments such as temperature changes, or combinations of both. For this reason, it is critical to test the quality and performance of the clock synchronization when the network or device is subjected to the types of impairments expected in the real world.

Standards Testing

The ITU-T and other organizations define standards for testing and implementation of timing and synchronization over Ethernet networks. Testing according to these standards is often required to bring equipment to market, or to ensure interoperability of various network equipment and the networks where they will operate. As these next-generation networks continue to grow, the need for guidance from the standards bodies increases in importance.

Test Case: G.8261 – Testing Timing over Packet (Ordinary Clocks)

Overview

In a packet-based timing network, PDV in the network affects the ability of the slave device to recover a physical clock accurately. The quality of clock recovery by the slave in the presence of this type of impairment must be measured.

The Ixia Anue G.8261 and MEF-18 test suites for the Ixia Anue 3500 are specifically designed for evaluating the clock recovery performance of Circuit Emulation (CES) and Timing over Packet (ToP) solutions under a variety of real-world network conditions. The G.8261 test suite covers all 17 test cases and their various iterations as defined in ITU-T G.8261 (2008) Appendix VI. The MEF-18 test suite covers the eight test cases found within section 6 'Synchronization' of the MEF-18 test plan, which calls for the creation of Packet Delay Variation (PDV) scenarios. ToP technology (including CES) is very sensitive to the PDV and loss conditions found in packet switched networks. Therefore, it is critical to verify the performance of the clock recovery algorithms found within these devices against real-world PDV and loss conditions before deployment.

ITU-T G.8261 Appendix VI suggests that one way to accomplish this is to build a mock network in the lab. However, these mock networks have many shortcomings, which are overcome by using network emulation technology to create the PDV and loss conditions required for testing. Emulation is far more accurate, repeatable, and flexible compared with building a mock network.

The Anue G.8261 and MEF-18 test suites precisely recreate the PDV and loss conditions produced for each 'network scenario' (number of switches and disturbance load characteristics) described within each ITU-T G.8261 (2008) and MEF-18 test case.

ITU-T G.8261

ITU-T G.8261 specifies network wander limits for ToP (for example, IEEE 1588) or CES across an NGN packet based network. G.8261 (2008) describes 17 test cases within Appendix VI as a guideline to the industry for evaluating the clock recovery performance of both CES and ToP solutions. See Table 1 later in this book for a list of test cases. Metrics such as TIE, MTIE, and frequency accuracy are measured during testing for validation against G.823, G.824, and G.8261 requirements. Figure 2 shows the mock network described within G.8261 Appendix VI, which includes 10 Ethernet switches connected in series with disturbance load traffic generators. With the Ixia Anue 3500, network emulation replaces the 10 Ethernet switches and disturbance load traffic generators, and the timing measurements are made in real-time during the test.

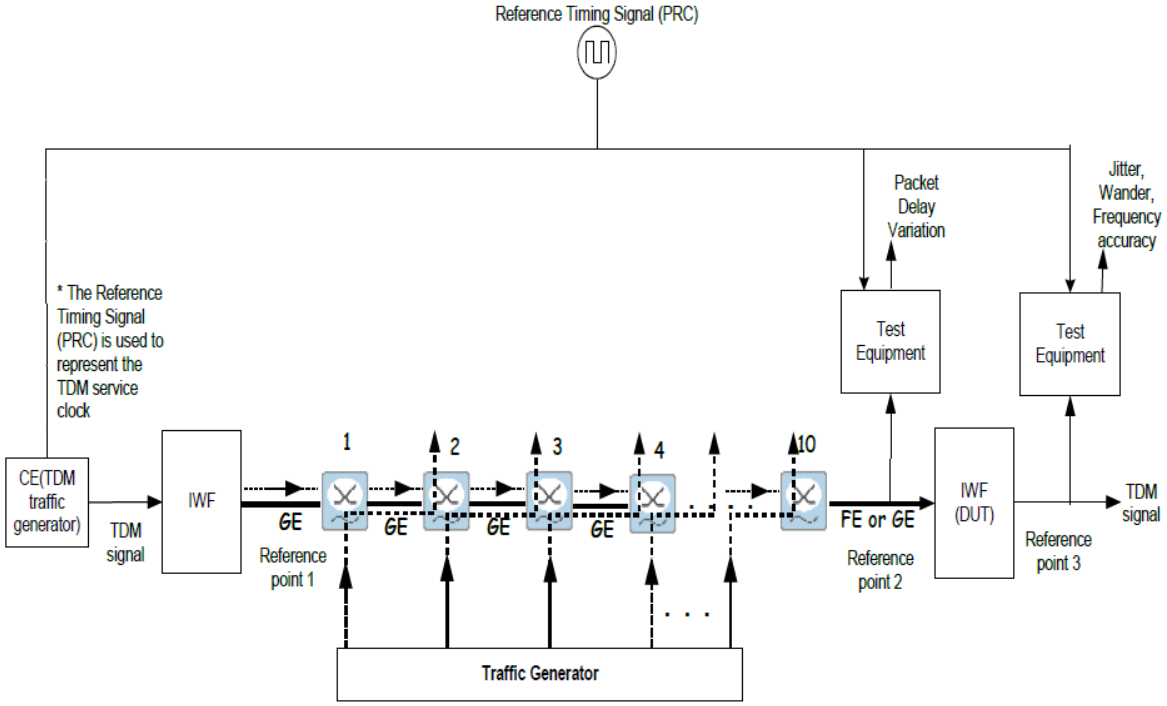


Figure 62. **ITU-T G.8261 Test Diagram – 10 switches in a Mock Network**

By using an Ixia Anue 3500 Network Emulator in place of the Ethernet switches as defined in the G.8261 Appendix VI Test Topology diagrams, tone can test against more realistic delay variation profiles and also create a highly repeatable test methodology.

MEF-18

Metro Ethernet Forum's MEF-18 defines abstract test procedures to verify that TDM services such as DS1, E1, DS3, and E3 that are transported over CES can be delivered with the required minimum output jitter and wander. MEF-18 certification testing is conducted by an officially endorsed test lab, and that lab uses network emulators running the Anue MEF-18 test suite. It is therefore advantageous for companies to pre-test their systems with the same test set up before formal MEF-18 certification testing. Table 1 contains a list of the test cases.

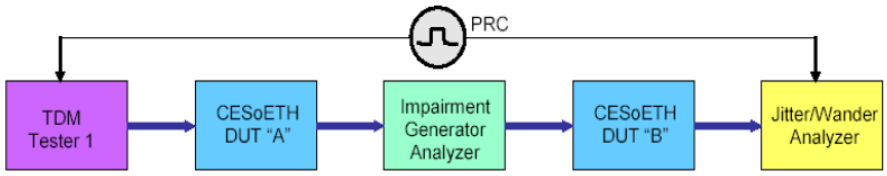


Figure 63. **EF-18 test bed as shown in MEF-18 test plan**

Description	**MEF-18** **'Test Case 6 – Synchronization'**	**ITU-T G.8261 Appendix VI** **April 2008**
Static Packet Load	NA	Test Case 1 (VI.3.2.2)
Sudden large network load changes – 80 % to 20 %	6.1 Only Traffic Model 2 (TM2)	Test Case 2 (VI.3.2.3)
Slow long timescale changes in network load – 1 % steps, 20 % to 80 %	6.2 Only TM2	Test Case 3 (VI.3.2.4)
Temporary network outages (10s shorter outage)	6.3 10 sec outage and TM2	Test Case 4 (VI.3.2.5)
Temporary network outages (100s longer outage)	Temporary network outages (100s longer outage)	Temporary network outages (100s longer outage)
6.4 100 sec outage and TM2	6.4 100 sec outage and TM2	6.4 100 sec outage and TM2
Test Case 4 (VI.3.2.5)	Test Case 4 (VI.3.2.5)	Test Case 4 (VI.3.2.5)
Temporary 100 % network congestion (10s shorter disturbance)	Temporary 100 % network congestion (10s shorter disturbance)	Temporary 100 % network congestion (10s shorter disturbance)
6.5 10 sec disturbance and TM2	6.5 10 sec disturbance and TM2	6.5 10 sec disturbance and TM2
Test Case 5 (VI.3.2.6)	Test Case 5 (VI.3.2.6)	Test Case 5 (VI.3.2.6)
Temporary 100 % network congestion (100s longer disturbance)	Temporary 100 % network congestion (100s longer disturbance)	Temporary 100 % network congestion (100s longer disturbance)
Route changes caused by network failure (small change)	Route changes caused by network failure (small change)	Route changes caused by network failure (small change)
6.7 Bypass 1 switch and TM2	6.7 Bypass 1 switch and	6.7 Bypass 1 switch and

Description	MEF-18 'Test Case 6 – Synchronization'	ITU-T G.8261 Appendix VI April 2008
	TM2	TM2
Test Case 6 (VI.3.2.7)	Test Case 6 (VI.3.2.7)	Test Case 6 (VI.3.2.7)
Route changes caused by network failure, 40 % load	Route changes caused by network failure, 40 % load	Route changes caused by network failure, 40 % load
6.8 Bypass 5 switches and TM2	6.8 Bypass 5 switches and TM2	6.8 Bypass 5 switches and TM2
Differential clock recovery method with noise added	NA	Test Case 10 (VI.4.2)
Differential clock recovery method with temporary network congestion	NA	Test Case 11 (VI.4.3)
Network disturbance load with 80 % forward direction, 20 % reverse	NA	Test Case 12 (VI.5.2.2)
Sudden large and persistent changes in network load	NA	Test Case 13 (VI.5.2.3)
Slow change in network load over an extremely long timescale	NA	Test Case 14 (VI.5.2.4)
Test temporary network outages and restoration	NA	Test Case 15 (VI.5.2.5)
Test temporary network congestion and restoration	NA	Test Case 16 (VI.5.2.6)
Route changes caused by network failure, 40 % forward load and 30 % reverse	NA	Test Case 17 (VI.5.2.7)

Table 1 Comparison of G.8261 (2008) and MEF-18 test cases

Details of these requirements are available in the following standards:

Recommendation ITU-T G.8261: Timing and synchronization aspects in packet networks

MEF-18: Abstract Test Suite for Circuit Emulation Services over Ethernet based on MEF 8

Objective

G.8261 testing is accomplished by measuring wander (low frequency phase variation) on the recovered clock interface of the slave or Ordinary Clock (DUT), while the specified packet impairment is applied inline between the Grand Master Clock and the Ordinary Clock. The Ixia Anue 3500 and the Grand Master Clock are provided with a common reference clock; normally, this is a clock signal sent to the 3500 from the Grand Master Clock over 2.048MHz BNC, 10MHz BNC, T1 BITS RJ48C, or E1 MTS RJ48C.

The testing is accomplished by measuring the recovered clock on the slave DUT while the specified impairment is being introduced between the Grand Master and the DUT.

For additional details, see ITU-T G.8261, Appendix VI *Measurement guidelines for packet-based methods*.

Setup

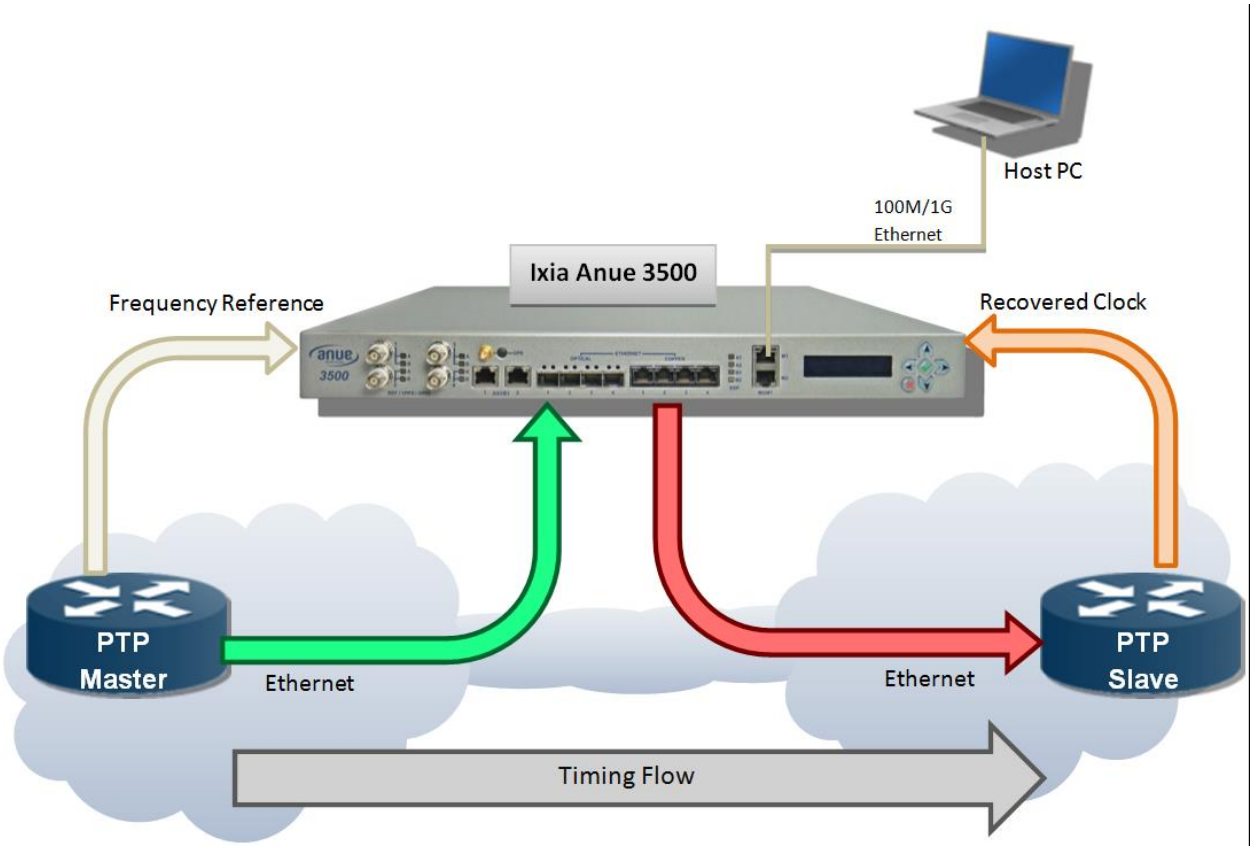
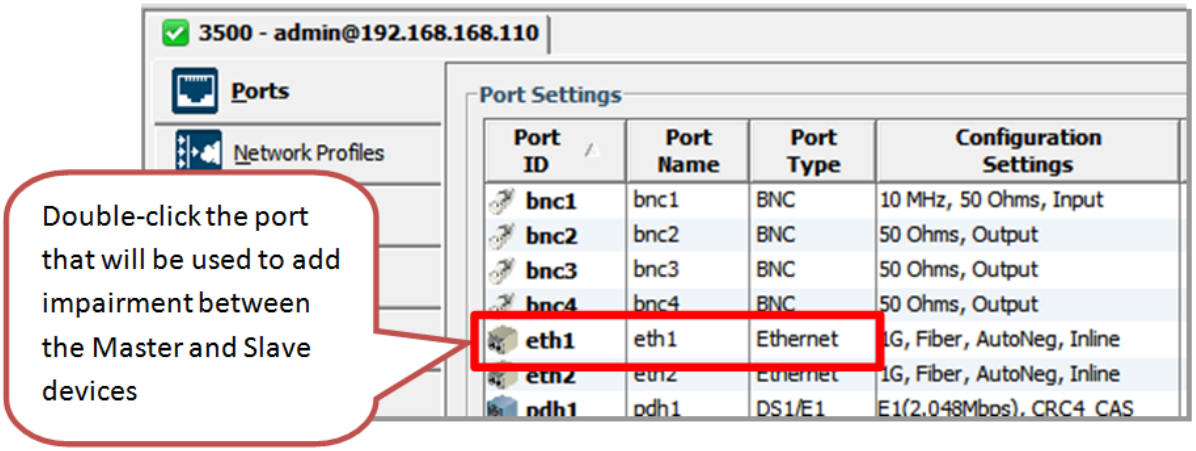
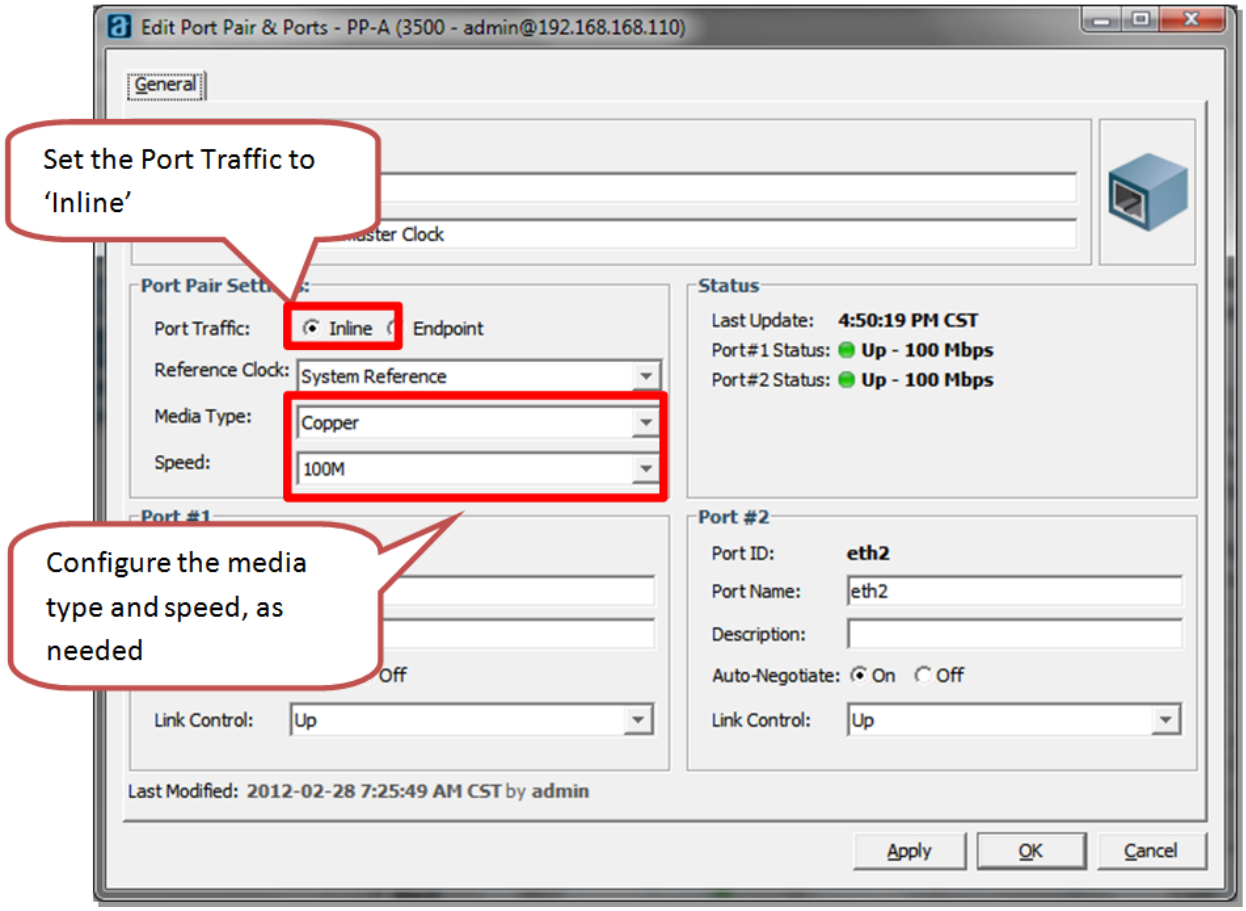


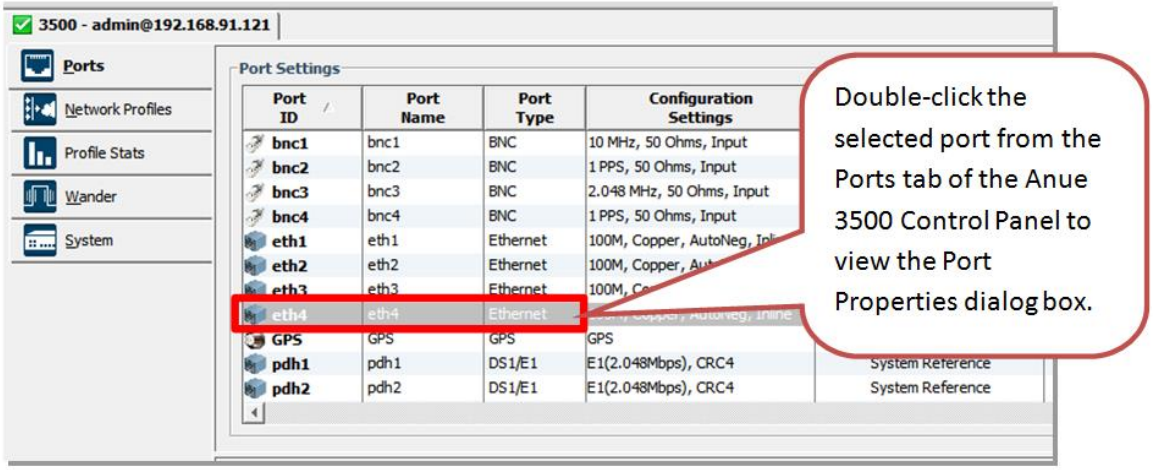
Figure 64. G.8261 Test Setup

1. Ensure that the Anue 3500 and the Grand Master Clock are connected to a common frequency reference.
2. Configure a port-pair on the Anue 3500 for 'Inline' mode, and if using 1G dual-media ports, configure for the correct media type and speed (copper or fiber, 100M or 1G) by using the Anue 3500 Control Panel Ports tab. Double-click the port that will be connected to the Grand Master Clock's Ethernet port. This brings up the Ethernet Port Property dialog box.

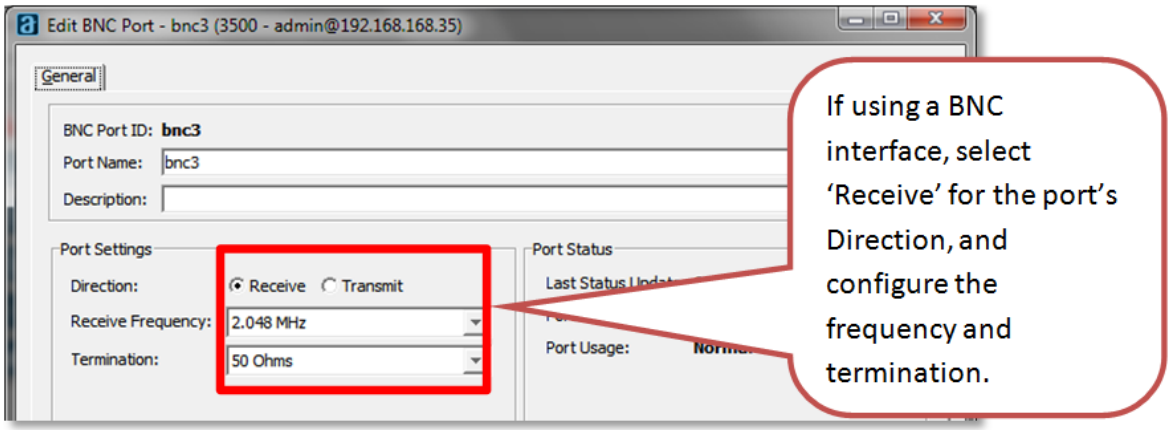


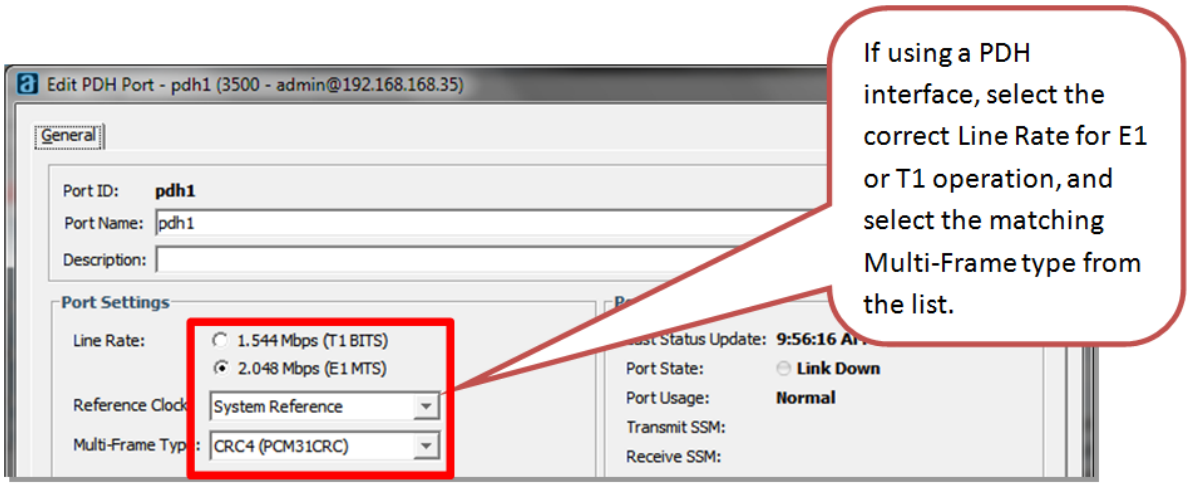


3. Connect the Grand Master Clock's Ethernet port to Eth1 and connect the Slave (DUT) Ethernet port to Eth2 (use Xeth1 and Xeth2 for 10G). Note the port that is connected to the Grand Master and the port that is connected to the Slave, to correctly configure the Network Profiles.

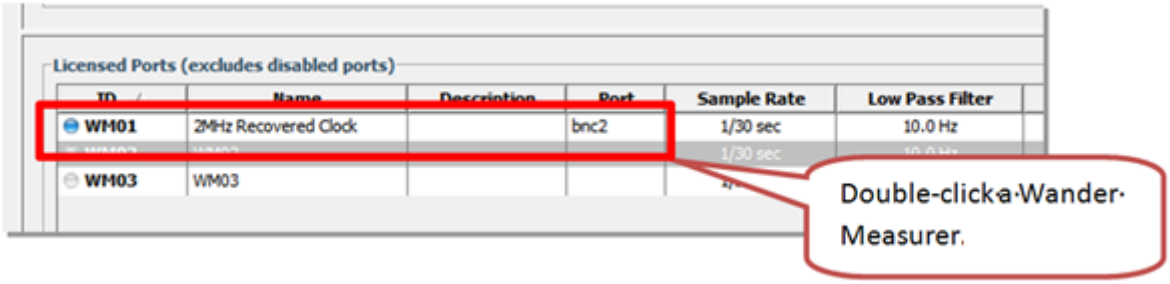


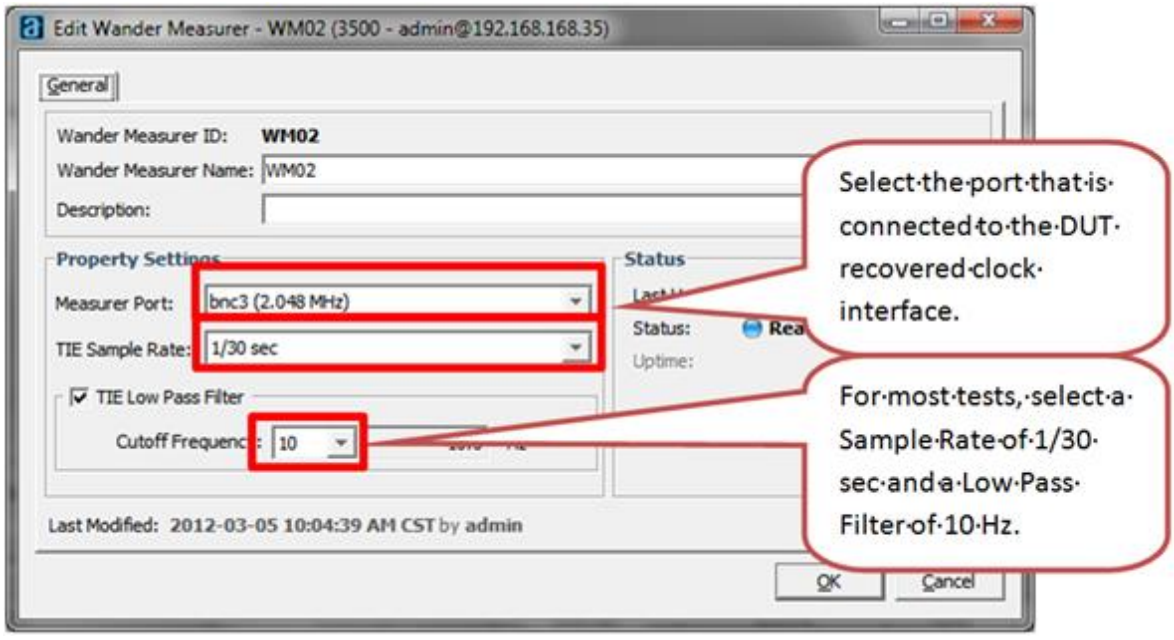
4. Connect the Slave's recovered clock interface to the 3500 by using the appropriate interface (BNC or PDH). Configure this interface to match the frequency and framing of the DUT's interface that is to be measured.



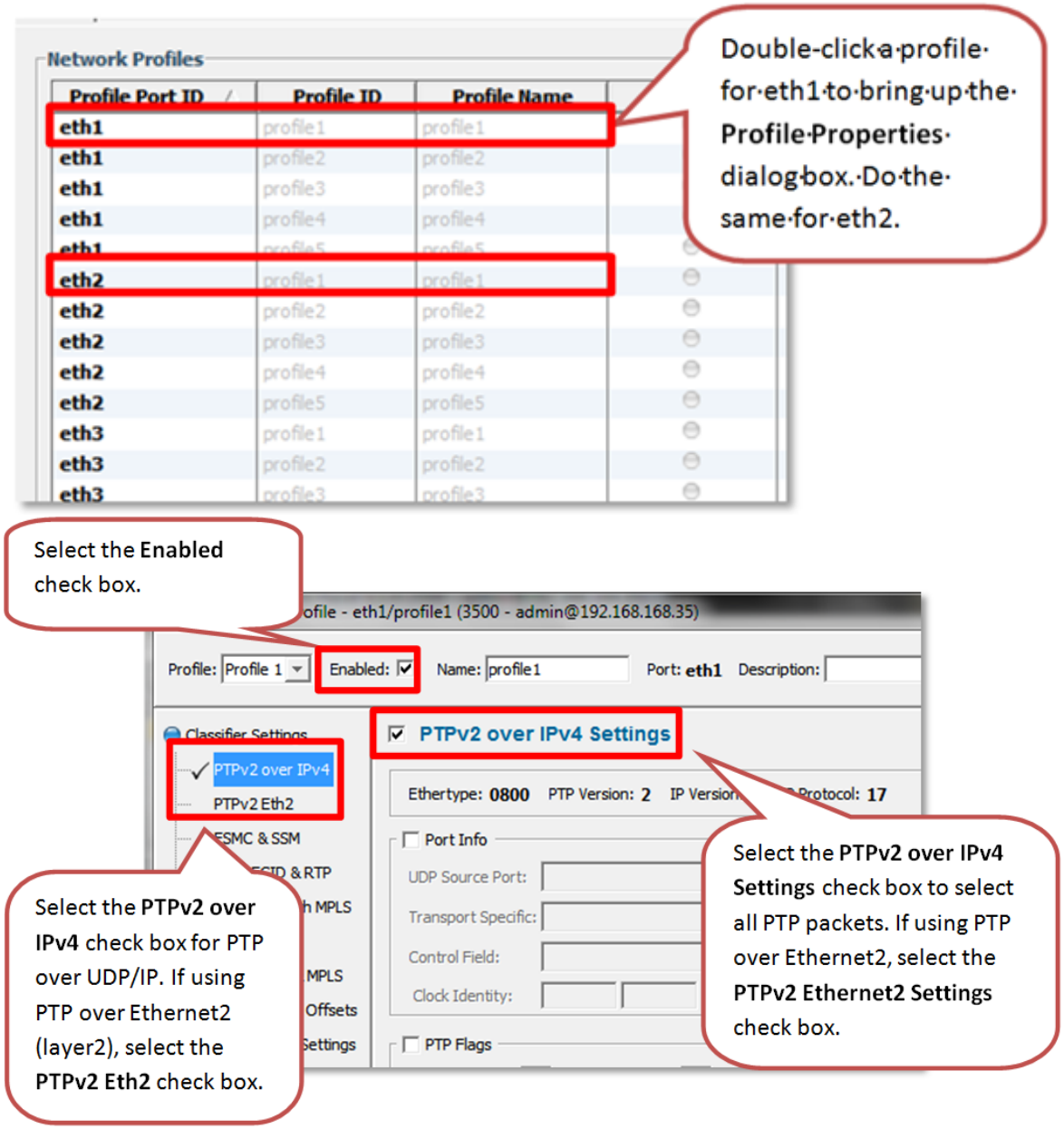


5. Select a Wander Measurer from the Anue 3500 Control Panel's Wander tab to measure the recovered clock interface. Configure the Wander Measurer for the correct interface.

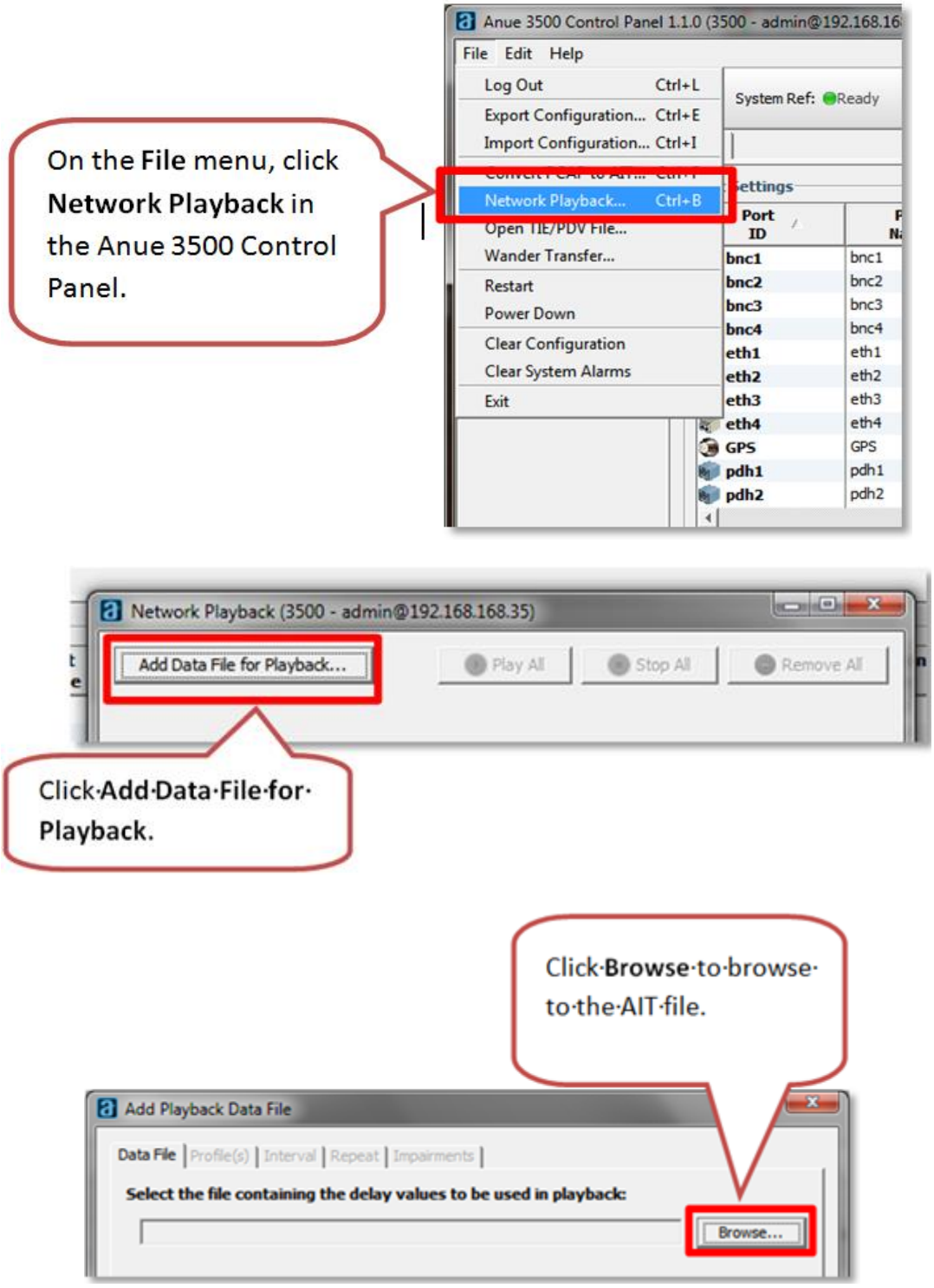


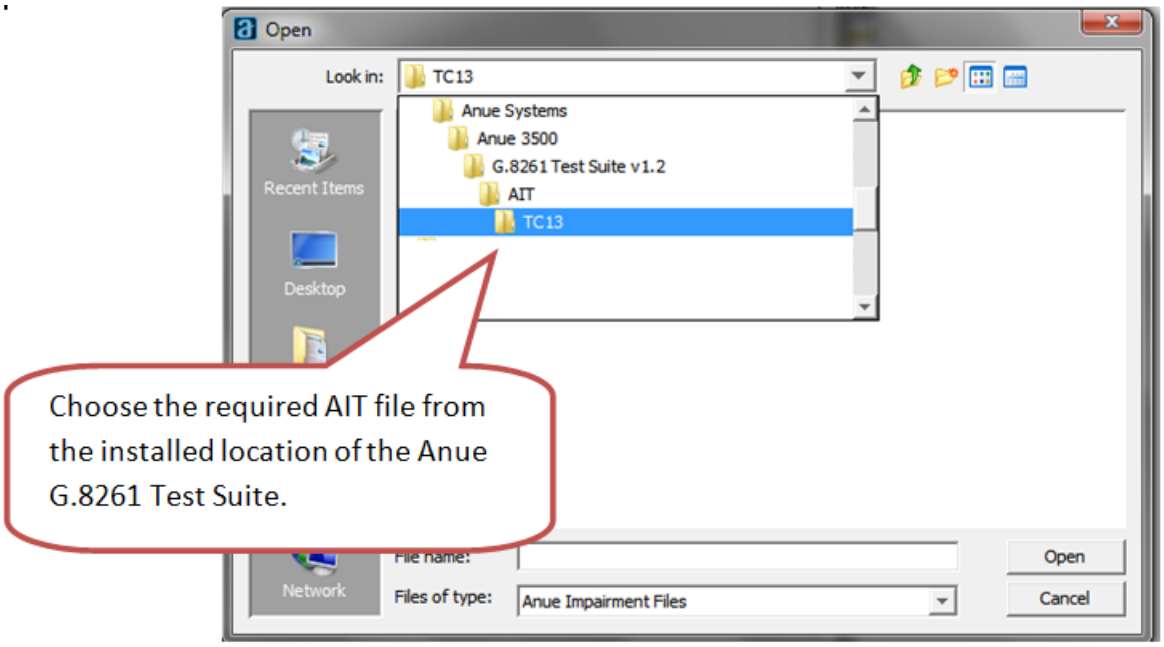


6. Configure Network Profiles for each port used in the test to match the PTP packets. Configure the classifier for PTP for each eth1 and eth2.
   ***Note**: You must do this procedure for both the port connected to the DUT as well as the port connected to the Grand Master Clock.*



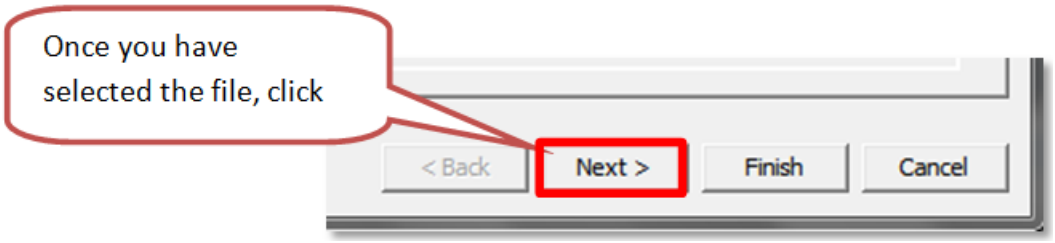
7. Load the impairments for the test case that is to be run.

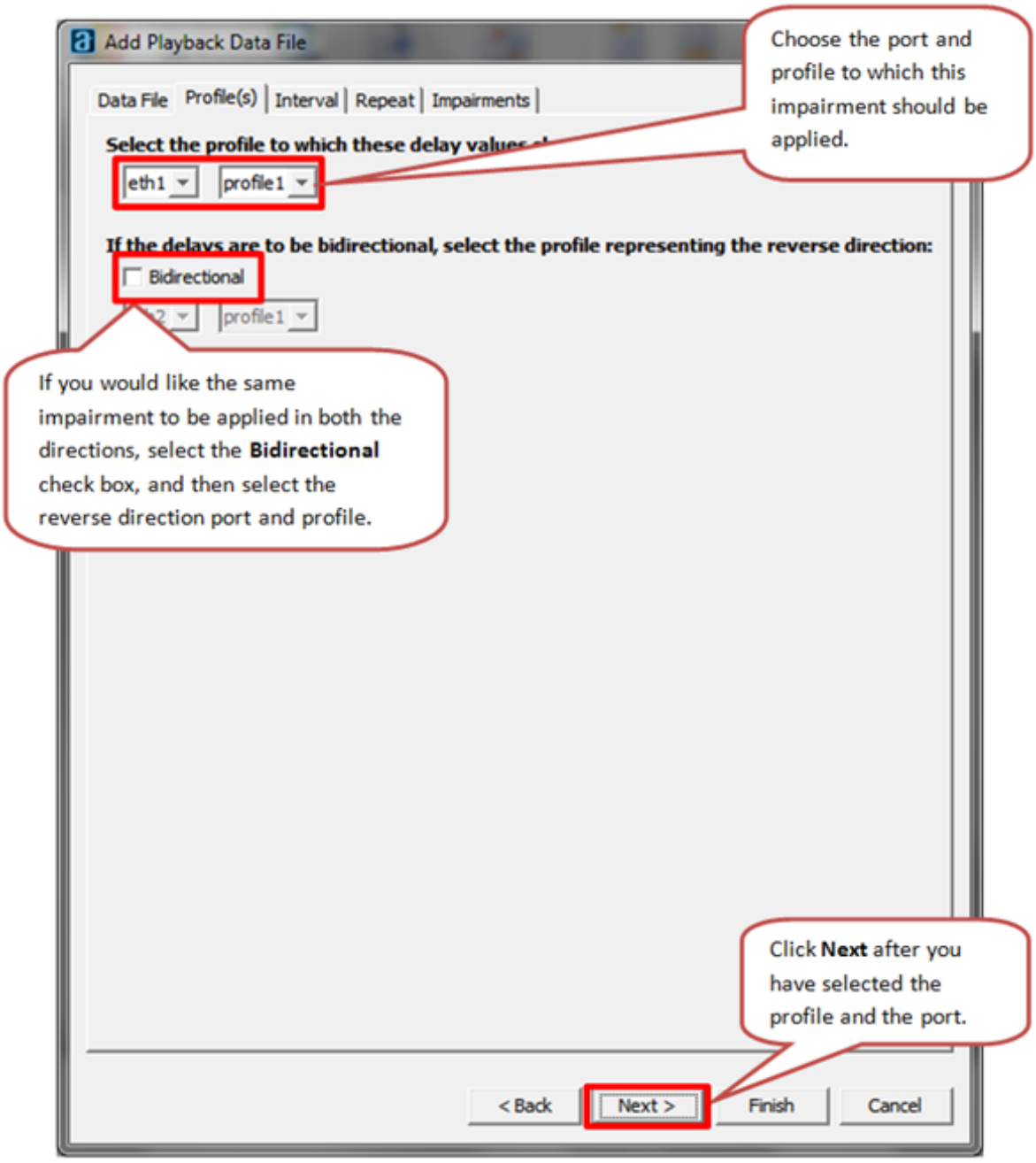


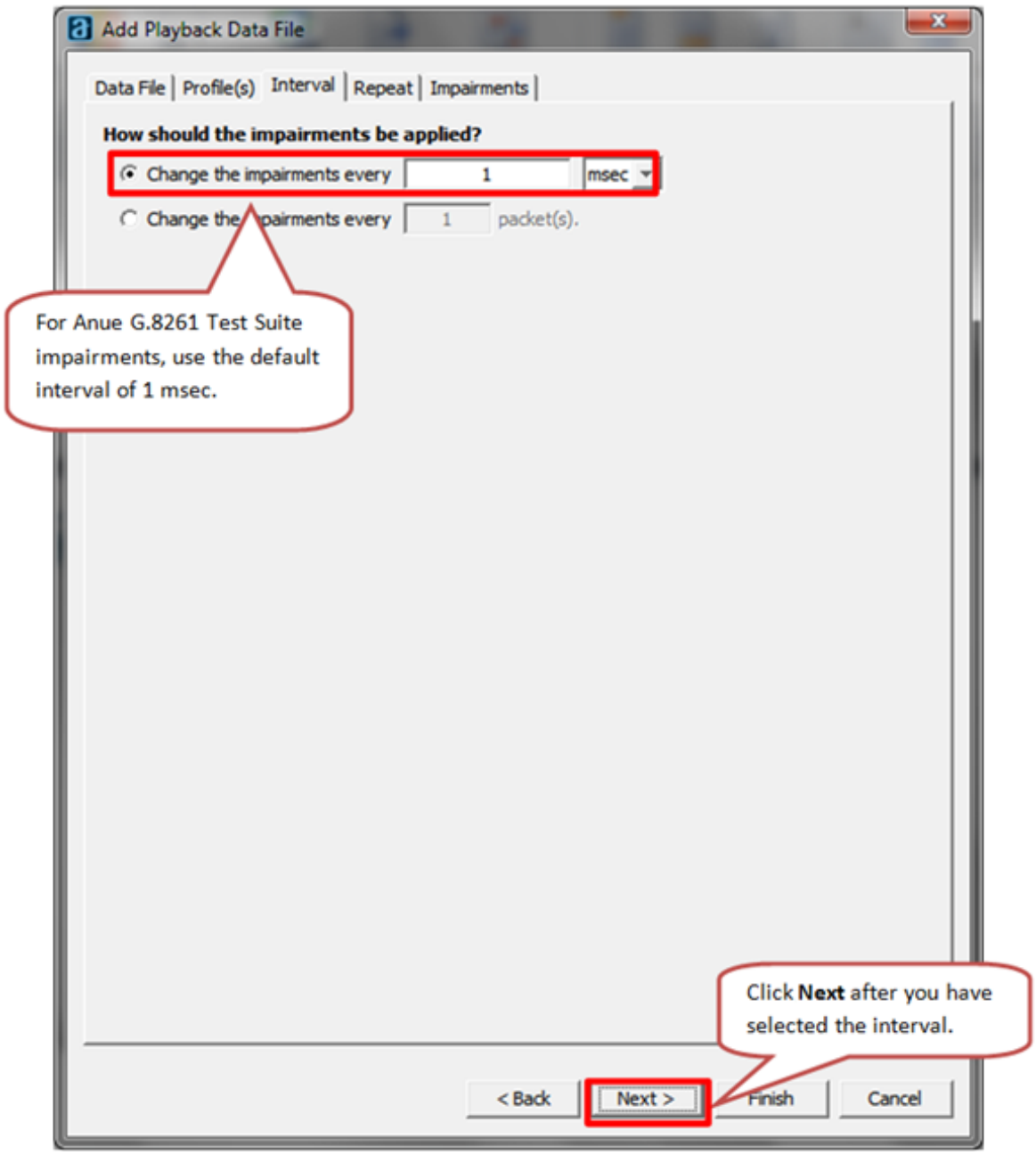


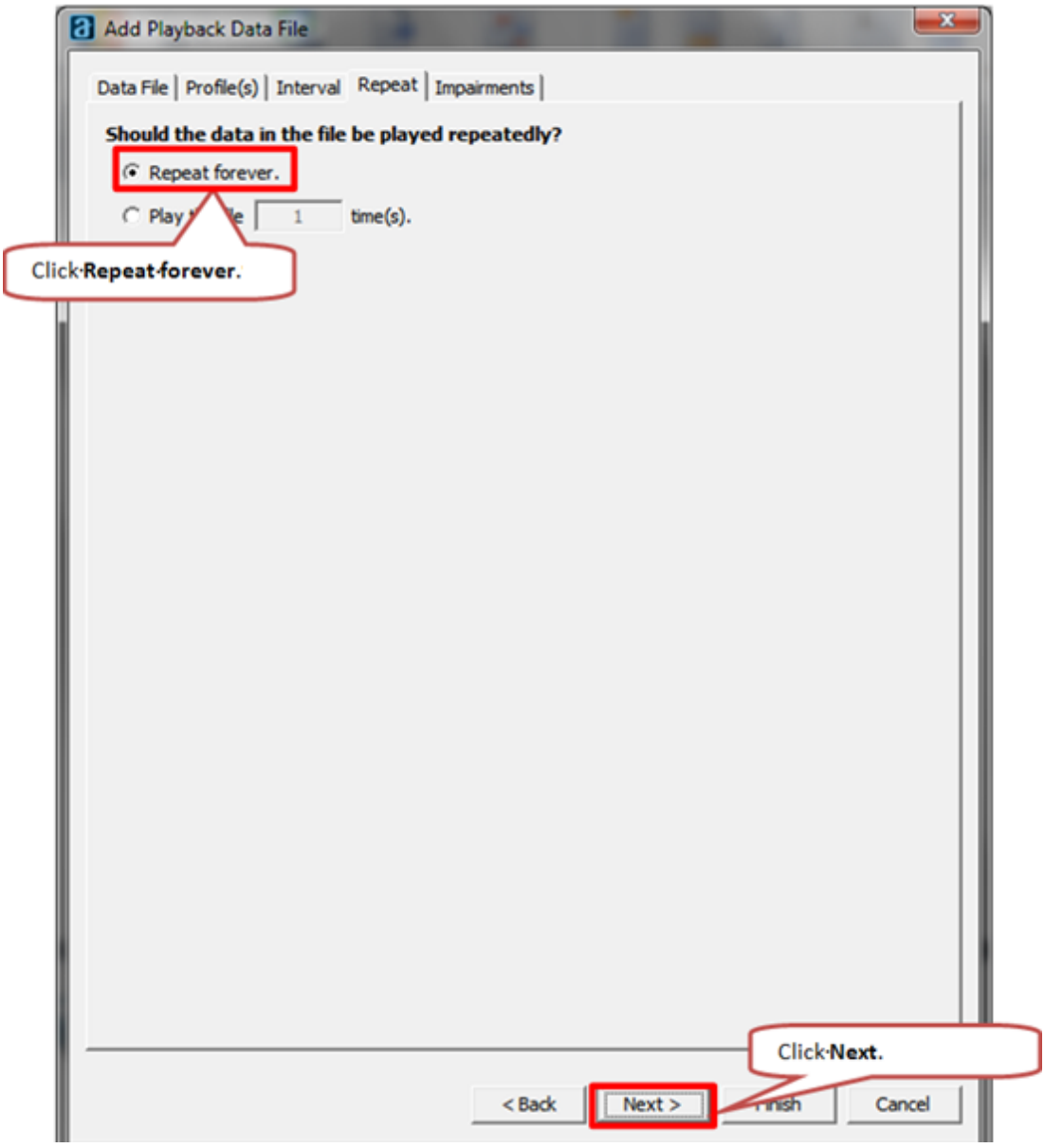
***Note**: The Anue G.8261 Test Suite must be installed on the computer before running these impairments. The files are normally installed in the user folder, for example, C:\users\username\Anue Systems\Anue 3500\G.8261 Test Suite v1.2\AIT\TC*nn*, where 'TC*nn*' refers to the test case. They are organized by number. For example, for Test Case 17, load 'TC17.'*

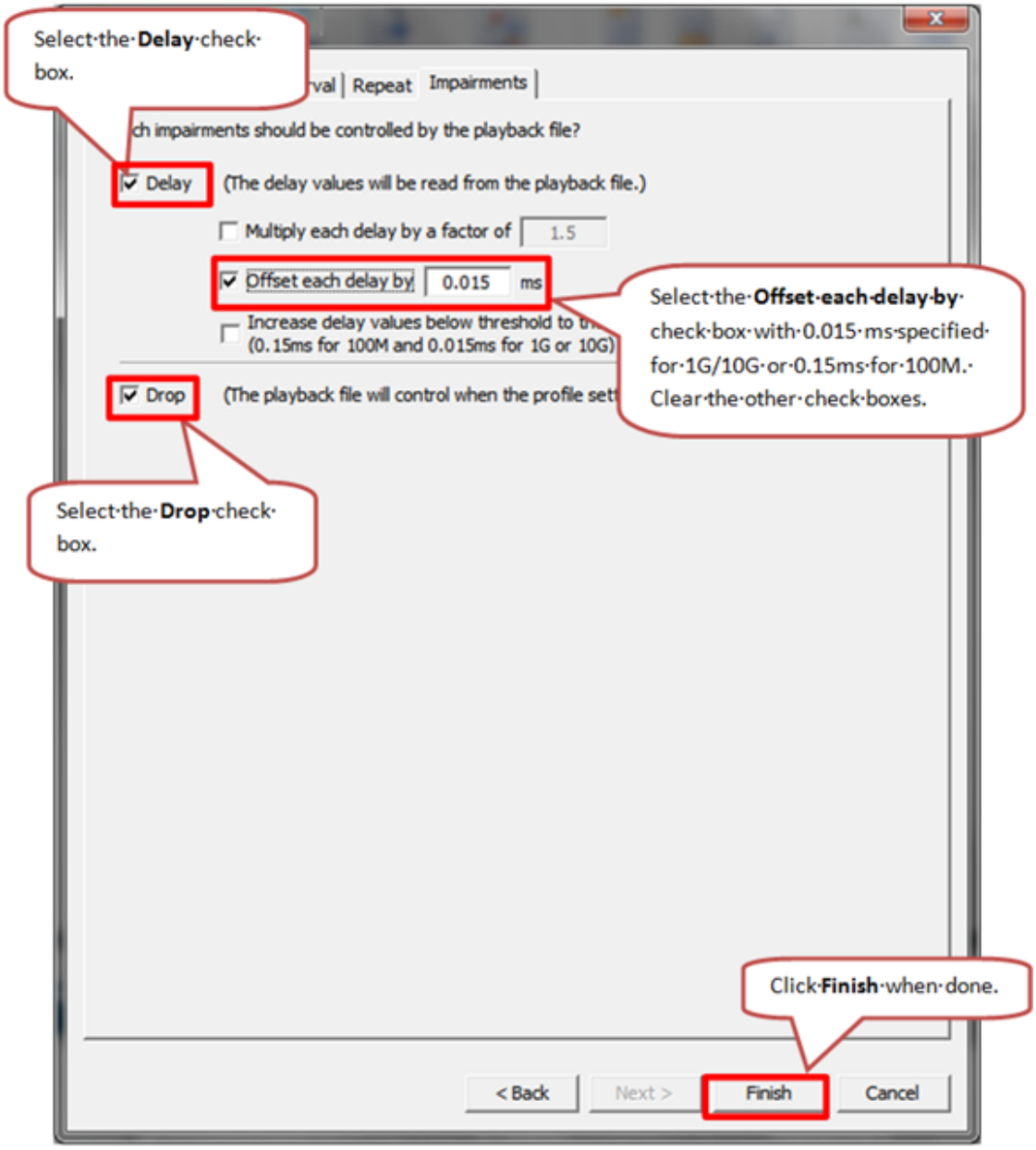
For bidirectional tests, there will be a "_fwd" and a "_rev" file. Use the "_fwd" file on the profile for the port connected to the DUT slave device, and use the "_rev" file on the profile for the port connected to the Grand Master Clock.

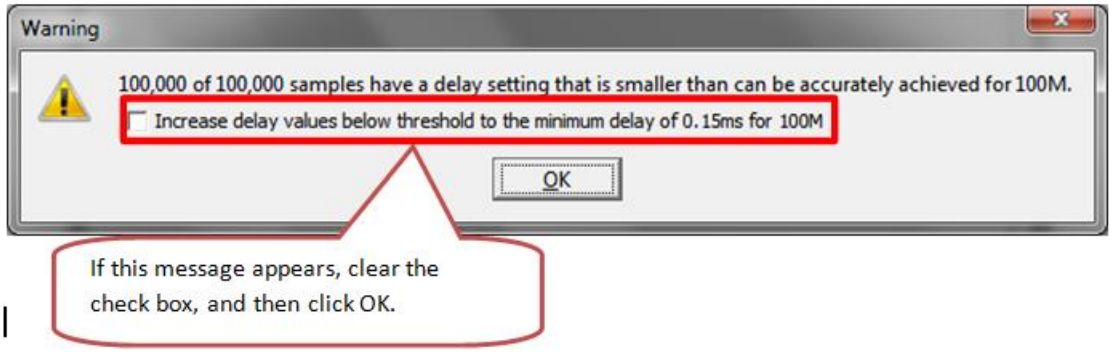



Add Playback Data File
Data File
Profile(s)
Interval
Repeat
Impairments
Select the profile to which these delay values
eth1
profile1
If the delays are to be bidirectional, select the profile representing the reverse direction:
Bidirectional
profile1
< Back
Next >
Finish
Cancel
Choose the port and profile to which this impairment should be applied.
If you would like the same impairment to be applied in both the directions, select the Bidirectional check box, and then select the reverse direction port and profile.
Click Next after you have selected the profile and the port.

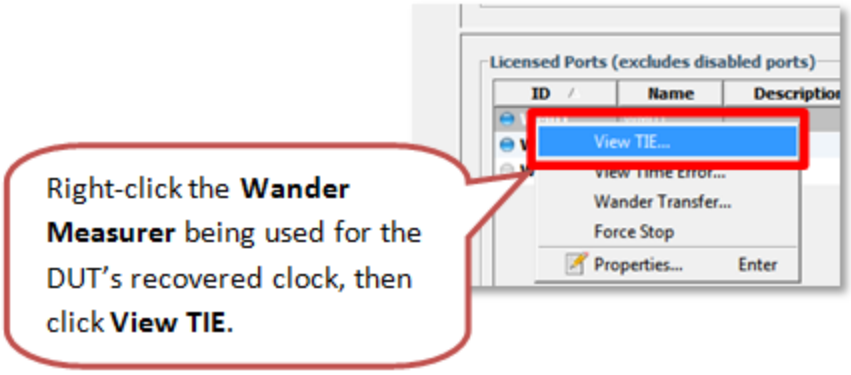

Add Playback Data File
Data File
Profile(s)
Interval
Repeat
Impairments
How should the impairments be applied?
Change the impairments every
1
msec
Change the pairments every
1
packet(s).
For Anue G.8261 Test Suite impairments, use the default interval of 1 msec.
Click Next after you have selected the interval.
< Back
Next >
Finish
Cancel

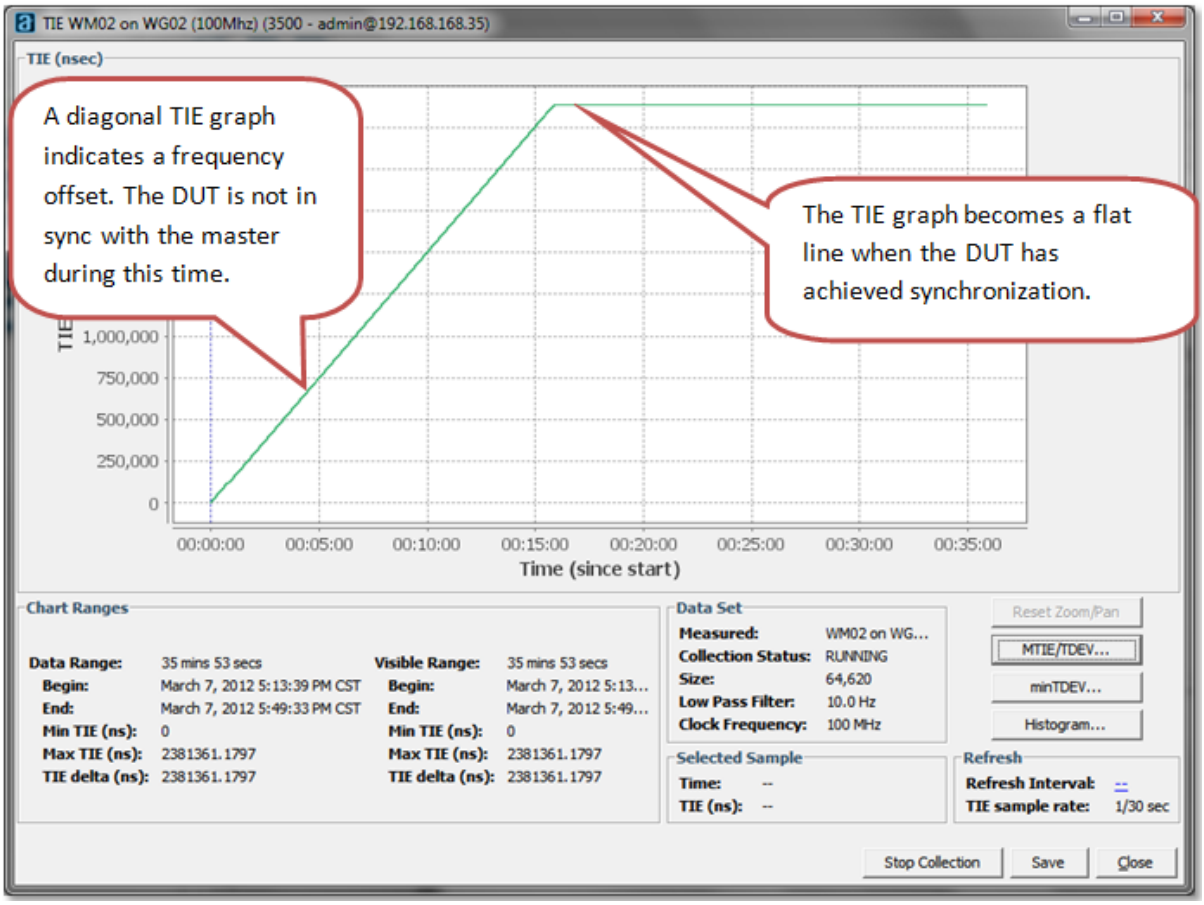

Add Playback Data File
Data File
Profile(s)
Interval
Repeat
Impairments
Should the data in the file be played repeatedly?
Repeat forever.
1
time(s).
Click Repeat forever.
Click Next.
< Back
Next >
Cancel


Select the Delay check box.
Repeat
Impairments
ch impairments should be controlled by the playback file?
Delay
(The delay values will be read from the playback file.)
Multiply each delay by a factor of
1.5
Offset each delay by
0.015
ms
Increase delay values below threshold to
(0.15ms for 100M and 0.015ms for 1G or 10G)
Drop
(The playback file will control when the profile set
Select the Offset each delay by check box with 0.015 ms specified for 1G/10G or 0.15ms for 100M. Clear the other check boxes.
Select the Drop check box.
Click Finish when done.
< Back
Next >
Finish
Cancel

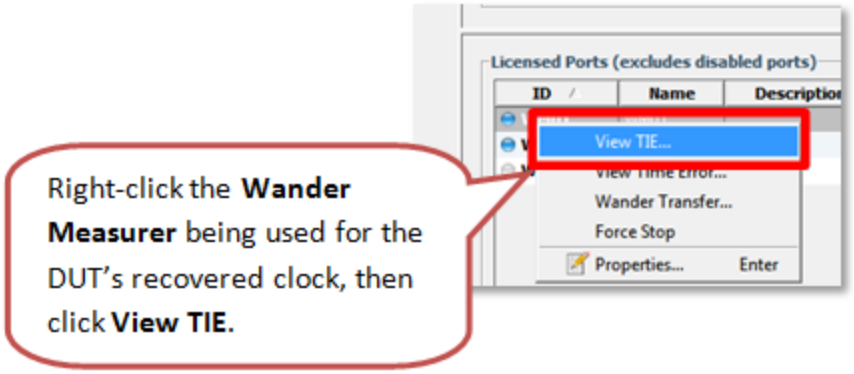


8. The PTP Slave DUT may take up to an hour or longer to synchronize with the Grand Master Clock. You can identify synchronization by monitoring the DUT's recovered clock TIE graph, and also by monitoring the user interface for indication of synchronization.



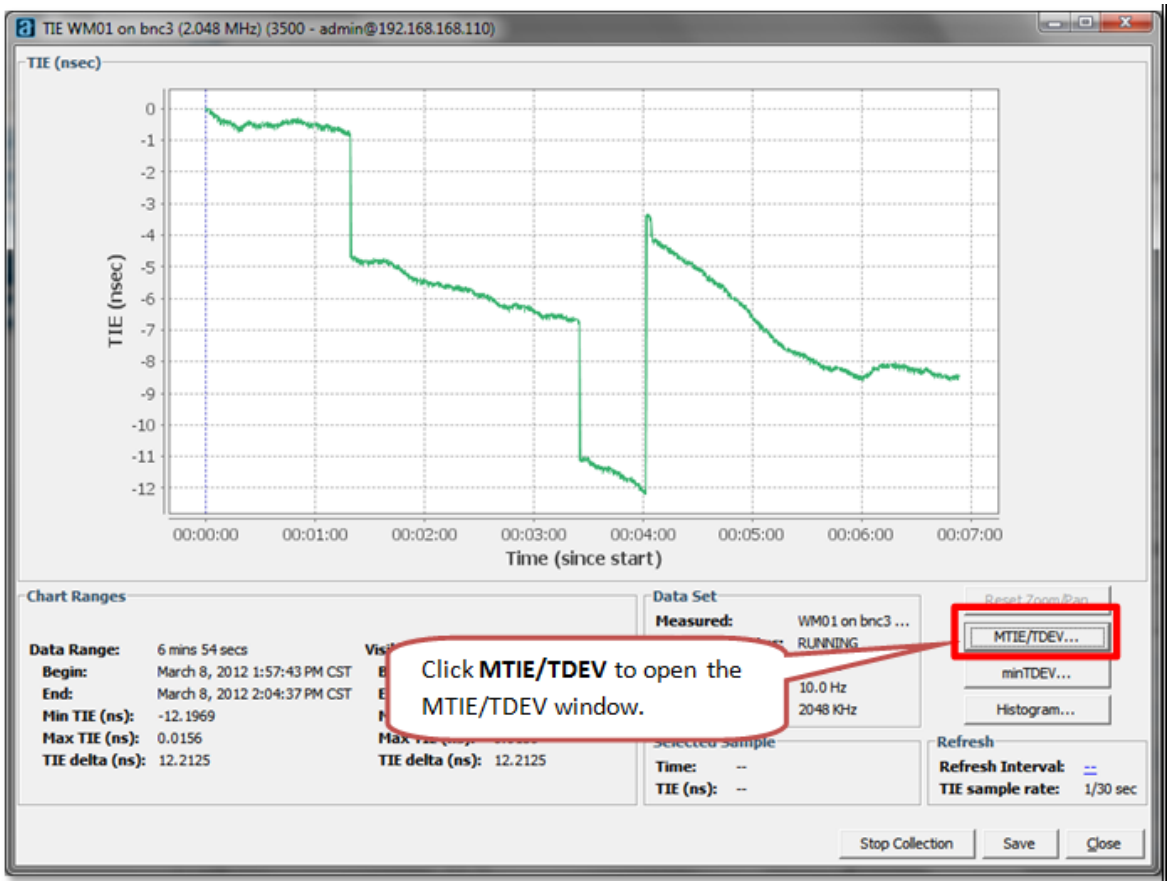

TIE WM02 on WG02 (100Mhz) (3500 - admin@192.168.168.35)
TIE (nsec)
A diagonal TIE graph indicates a frequency offset. The DUT is not in sync with the master during this time.
The TIE graph becomes a flat line when the DUT has achieved synchronization.
TIE
1,000,000
750,000
500,000
250,000
0
00:00:00
00:05:00
00:10:00
00:15:00
00:20:00
00:25:00
00:30:00
00:35:00
Time (since start)
Chart Ranges
Data Range: 35 mins 53 secs
Begin: March 7, 2012 5:13:39 PM CST
End: March 7, 2012 5:49:33 PM CST
Min TIE (ns): 0
Max TIE (ns): 2381361.1797
TIE delta (ns): 2381361.1797
Visible Range: 35 mins 53 secs
Begin: March 7, 2012 5:13...
End: March 7, 2012 5:49...
Min TIE (ns): 0
Max TIE (ns): 2381361.1797
TIE delta (ns): 2381361.1797
Data Set
Measured: WM02 on WG...
Collection Status: RUNNING
Size: 64,620
Low Pass Filter: 10.0 Hz
Clock Frequency: 100 MHz
Selected Sample
Time: --
TIE (ns): --
Reset Zoom/Pan
MTIE/TDEV...
minTDEV...
Histogram...
Refresh
Refresh Interval: --
TIE sample rate: 1/30 sec
Stop Collection
Save
Close

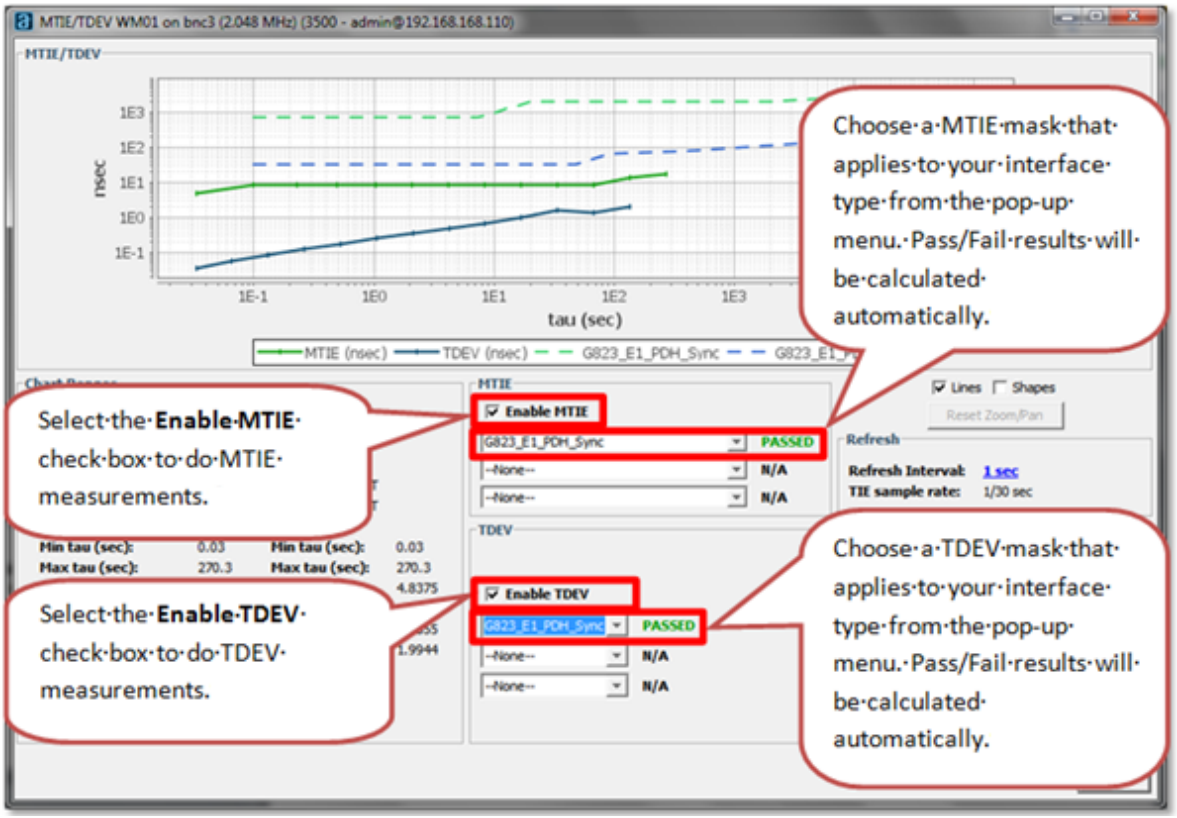
9. After the DUT is in sync with the Grand Master, close the TIE window and restart the TIE measurement.



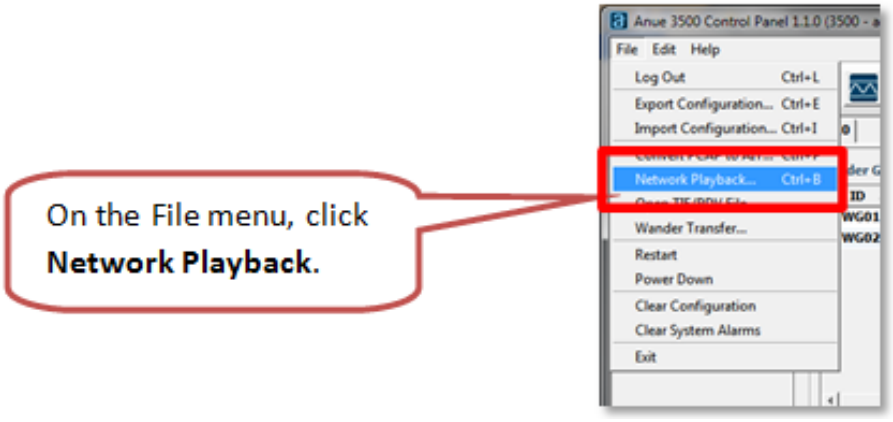
Step-by-Step Instructions

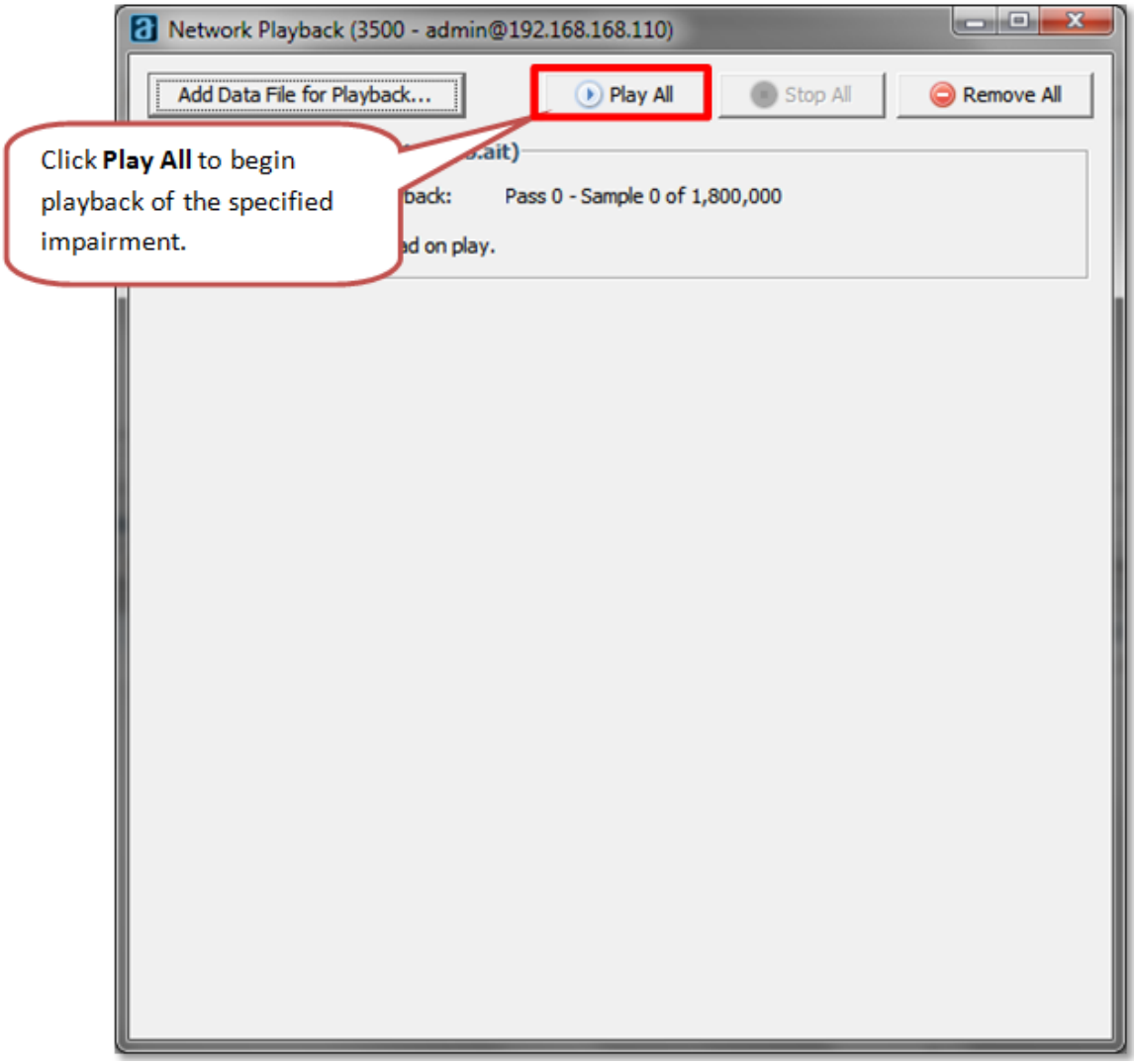
1. View the MTIE and TDEV results, including the Pass/Fail results against the masks that are applicable to your interface type by clicking **MTIE/TDEV** in the TIE graphical window.





2. Play the impairment by using Network Playback while keeping the TIE window open (recording TIE). You can also monitor the MTIE/TDEV results during the test.




Network Playback (3500 - admin@192.168.168.110)
Add Data File for Playback...
Play All
Stop All
Remove All
Click **Play All** to begin playback of the specified impairment.
Pass 0 - Sample 0 of 1,800,000

Test Variables

Repeat the test with the following variations:

- Test with **each G.8261 PDV profile** applicable to your equipment, or alternatively, **with each MEF-18 impairment profile.**
- Test each recovered clock interface according to the mask applicable to the interface, such as G.823 for E1 and G.8262 for SyncE.
- Test each interface in multiple modes, such as T1 and E1 or framing modes.
- Test with the system in both PTP **multicast** mode and in PTP **unicast** mode.
- Test with the system in both **one-step mode** (which reduces the number of messages) and in **two-step mode**.
- Test using varying sync and follow-up packet rates and different PTP profiles, if supported.
- Test multiple Ethernet speeds and on all supported interfaces (10G, 1G, copper/optical).

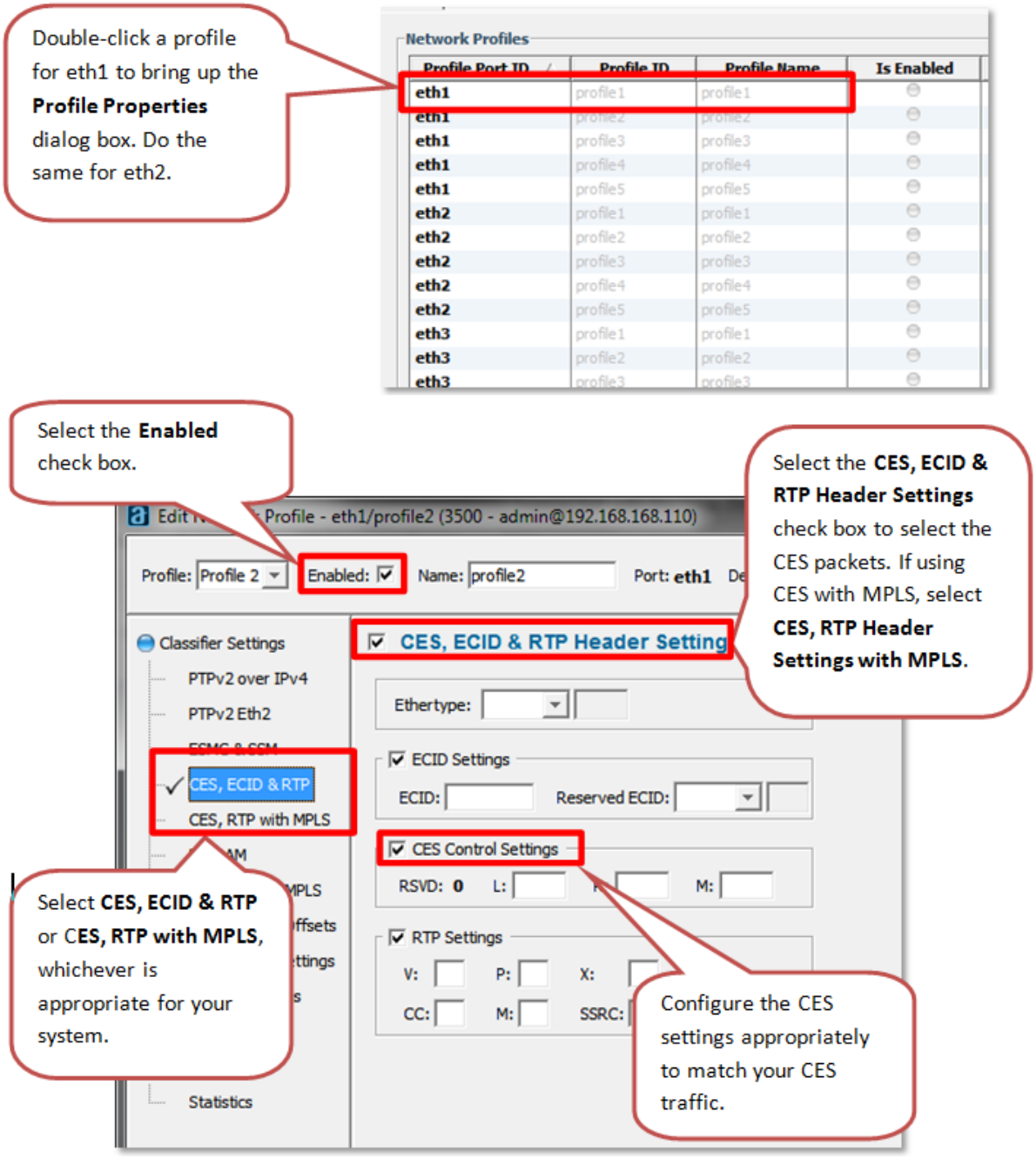
Test Variable using G.8261 Test Cases 1-17 with CES

Timing over Packet networks may use Circuit Emulation Services (CES). CES uses equipment known as Interwork Framework devices (IWF) to transport TDM interface traffic such as T1 or E1 across asynchronous Ethernet packet networks.

TDM circuits send traffic at a constant frame rate from one interface to the next. Because these frames are sent at a constant known rate, it is not necessary to use timestamps to recover the clock. While the CES traffic is synchronous by nature, the intervening Ethernet packet network used for CES between the IWF devices is asynchronous, and therefore, the quality of frequency synchronization must be tested. The IWF devices (DUT) may have physical clock interfaces or may provide the clock along with data on the encapsulated TDM stream.

Testing of CES is essentially the same as PTP/IEEE 1588 testing with very minor variations, mostly with regard to how traffic is classified. The testing is accomplished by measuring the recovered clock or PDH interface on the slave DUT while the specified impairment is being introduced between the master and slave IWF device.

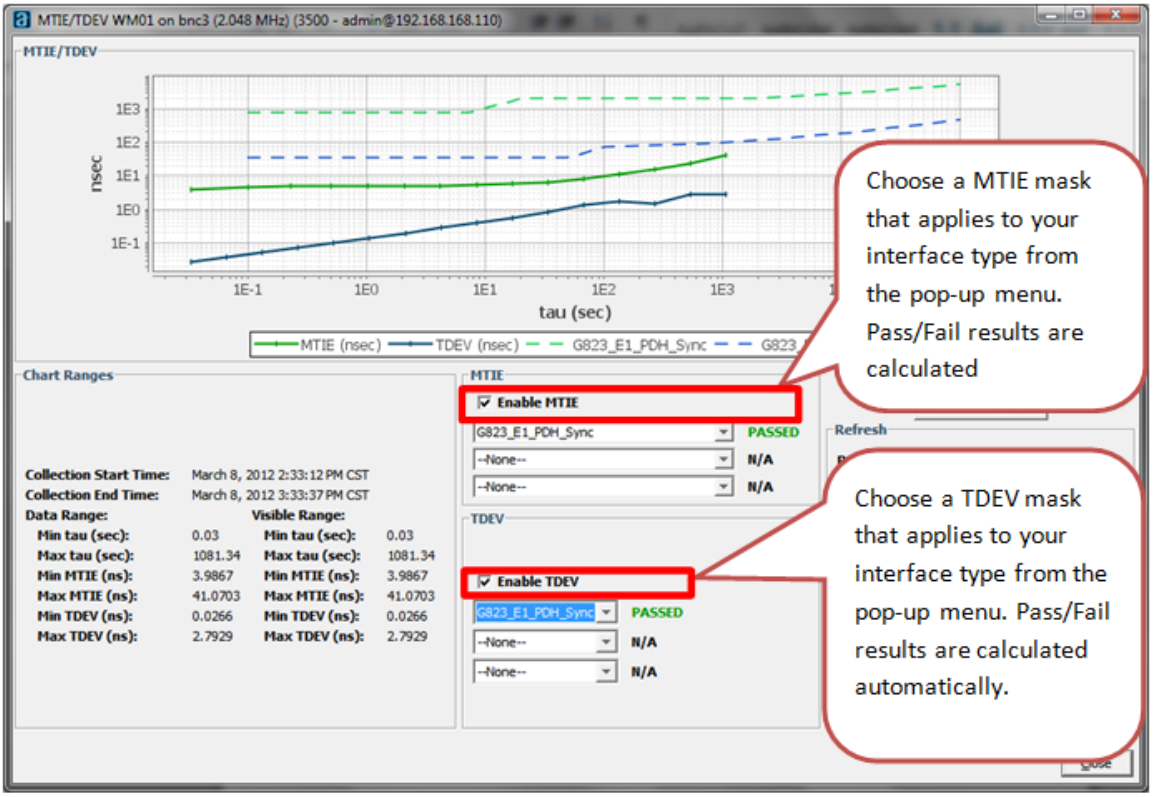
1. Follow the test setup steps in ’Testing Timing Over Packet (Ordinary Clocks)’ with the following variations:
   Configure Network Profiles for each port used in the test to match the CES packets. Configure the classifier for CES for each eth1 and eth2. *Note: You must do this procedure for both the port connected to the DUTslave IWF as well as the port connected to the Master IWF.*


Double-click a profile for eth1 to bring up the **Profile Properties** dialog box. Do the same for eth2.
Network Profiles
Profile Port ID
Profile ID
Profile Name
Is Enabled
eth1 profile1 profile1
eth1 profile2 profile2
eth1 profile3 profile3
eth1 profile4 profile4
eth1 profile5 profile5
eth2 profile1 profile1
eth2 profile2 profile2
eth2 profile3 profile3
eth2 profile4 profile4
eth2 profile5 profile5
eth3 profile1 profile1
eth3 profile2 profile2
eth3 profile3 profile3
Select the **Enabled** check box.
Profile - eth1/profile2 (3500 - admin@192.168.168.110)
Profile: Profile 2
Enabled:
Name: profile2
Port: eth1
Classifier Settings
PTPv2 over IPv4
PTPv2 Eth2
CES, ECID & RTP
CES, RTP with MPLS
Statistics
CES, ECID & RTP Header Setting
Ethertype:
ECID Settings
ECID:
Reserved ECID:
CES Control Settings
RSVD: 0
L:
M:
RTP Settings
V:
P:
X:
CC:
M:
SSRC:
Select the **CES, ECID & RTP Header Settings** check box to select the CES packets. If using CES with MPLS, select **CES, RTP Header Settings with MPLS**.
Select **CES, ECID & RTP** or **CES, RTP with MPLS**, whichever is appropriate for your system.
Configure the CES settings appropriately to match your CES traffic.

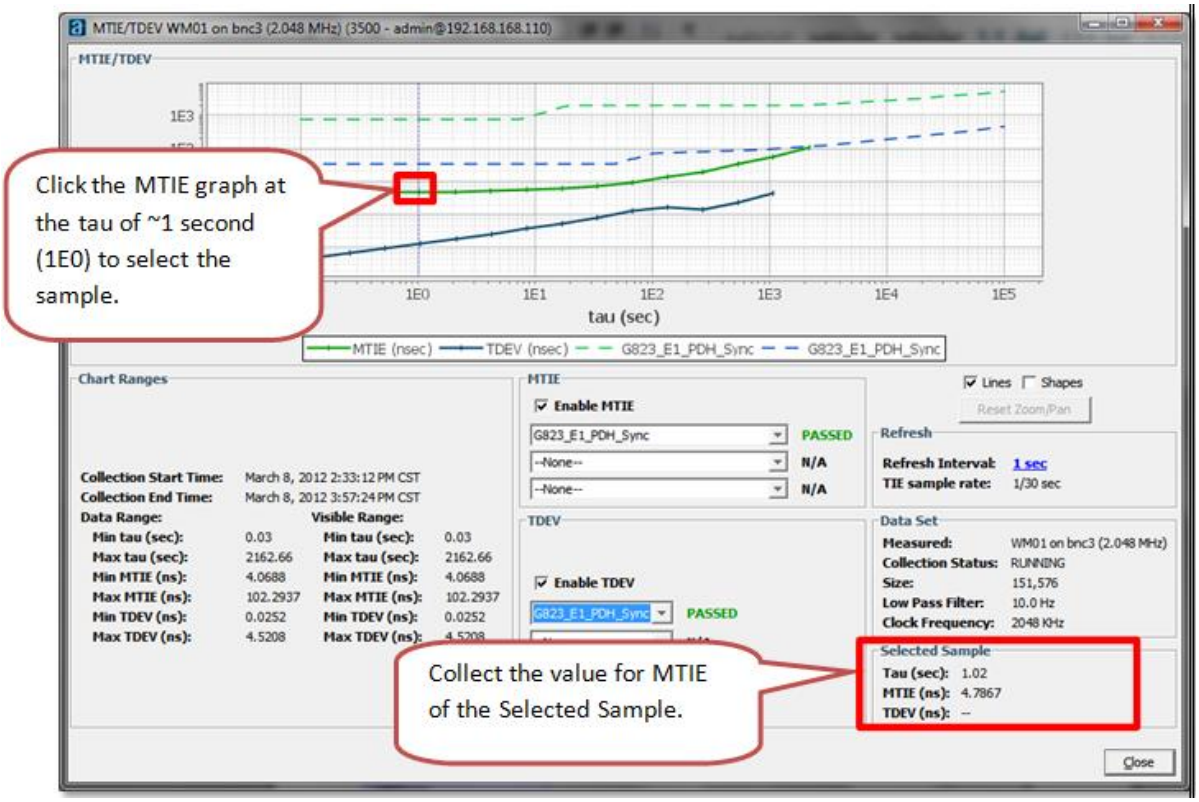
Results Analysis

1. Each test case includes an impairment that is specified for a certain length of time, ranging from a few minutes to several hours. The result data (TIE) must be collected during the duration of the impairment. After the impairment for the particular test case finishes, evaluate the frequency accuracy and stability in the MTIE/TDEV window. The graphs for MTIE and TDEV are plotted against the selected masks and pass/fail indication is provided for each mask that is selected.

Note: You must begin recording TIE data before you begin the impairment, and do not close the TIE window for the duration of the test. After you close the TIE window, the Anue 3500 will stop collecting the necessary TIE data for the results.



2. Evaluate the maximum frequency offset. Typically, the frequency offset is measured in terms of the MTIE value at a tau of 1 second. This can be evaluated in the MTIE/TDEV window by clicking the cursor on the MTIE plot at the tau closest to 1 second (1.02 seconds).



The MTIE is indicated in ns (nanoseconds). Frequency offset is typically expressed in ppb (parts per billion). The number of nanoseconds of MTIE at one second of tau is equivalent to ppb frequency offset. So, for example, in this measurement, the frequency offset is 4.7867ppb.

The maximum frequency offsets are defined by the relevant standard, which applies to the interface type. For example, ITU-T G.823 Table 14 defines the maximum frequency offset at traffic interfaces for E1.

Conclusions

Testing PTP / IEEE1588 performance according to G.8261 is an important industry-accepted standard that is critical to ensure network compatibility and interoperability.

G.8262 – Testing Synchronous Ethernet Equipment Clocks

As the demand for advanced mobile broadband services continues to increase, many network providers and carriers are migrating their mobile backhaul networks from legacy synchronous transports such as SONET/SDH and T1/E1 to Carrier Ethernet. To deliver synchronization services, Synchronous Ethernet (SyncE) is increasingly being used, alone or in conjunction with IEEE 1588 (precision time protocol, PTP). The need to test the providers' services and equipment on their new SyncE networks has emerged, and the ITU-T G.8262 standard provides applicable tests to verify that SyncE equipment and applications function correctly under a range of timing impairment conditions known collectively as 'wander.'

The Anue 3500 allows for comprehensive testing of Synchronous Ethernet (SyncE) as specified in ITU-T G.8262:

Test	Requirement
Wander Generation	ITU-T G.8262 Section 8 'Noise generation'
Wander Tolerance	ITU-T G.8262 Section 9 'Noise tolerance'
Wander Transfer	ITU-T G.8262 Section 10 'Noise transfer'
Transients and Holdover	ITU-T G.8262 Section 11 'Transient response and holdover performance'

Wander Generation refers to the phase noise that is introduced by the DUT alone, that is, the difference in phase between the input reference clock on the DUT and the SyncE recovered clock on the DUT's Ethernet output.

Wander Tolerance refers to the ability of the DUT to tolerate phase noise that is introduced by the physical network present between two SyncE devices.

Wander Transfer refers to the phase noise present on the DUT's input that is transmit to the SyncE Ethernet output or slave clock.

Details of these requirements are available in *Recommendation ITU-T G.8262 – Timing characteristics of a synchronous Ethernet equipment slave clock.*

Test Case: Wander Generation

Overview

An EEC must produce minimal output wander when synchronized to an ideal reference. ITU-T G.8262 provides testing parameters for wander generated by the EEC.

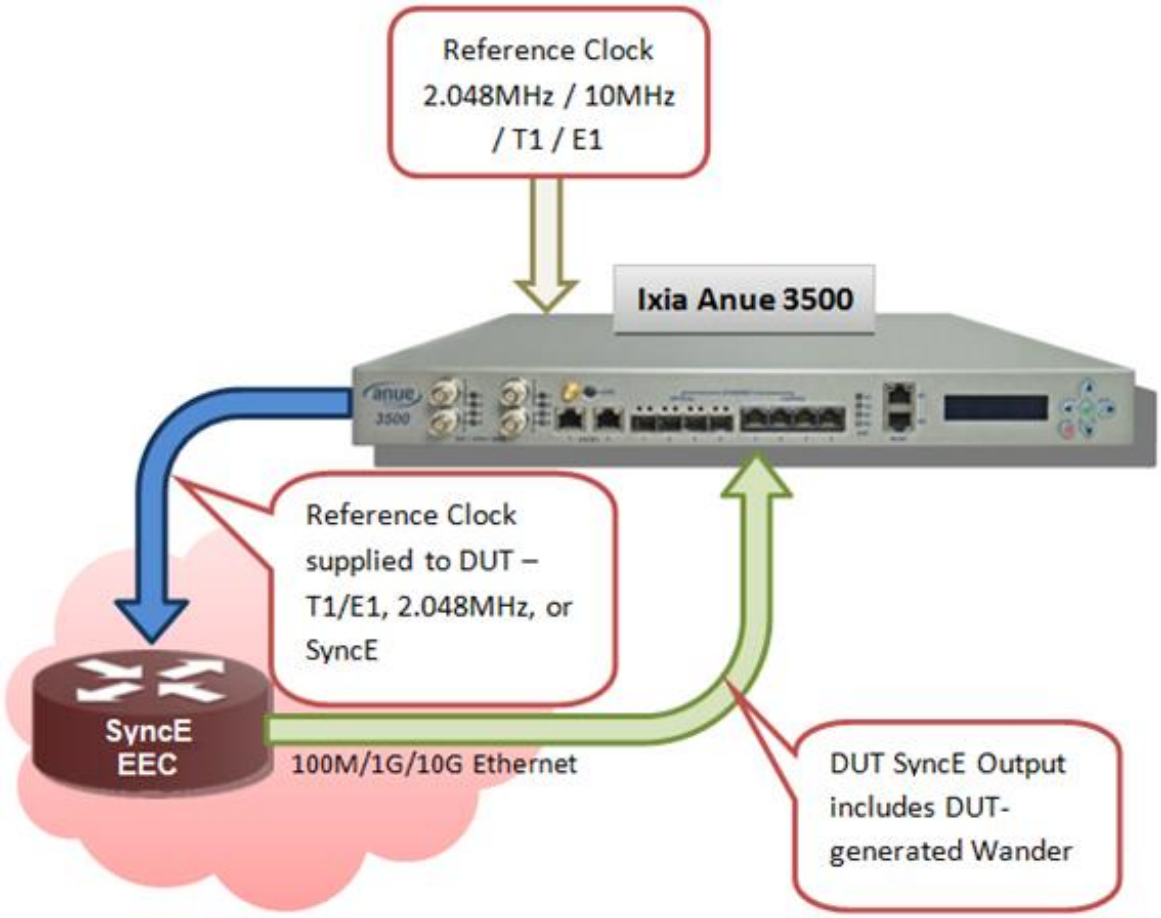
Objective

This test measures the wander (phase noise) present on the DUT's output when an ideal input reference signal is supplied by the Anue 3500. The difference in wander present on the DUT's output compared to the ideal input reference clock is the wander that is generated by the DUT. The wander generated by the DUT is measured in terms of Maximum Time Interval Error (MTIE) and Time Deviation (TDEV).

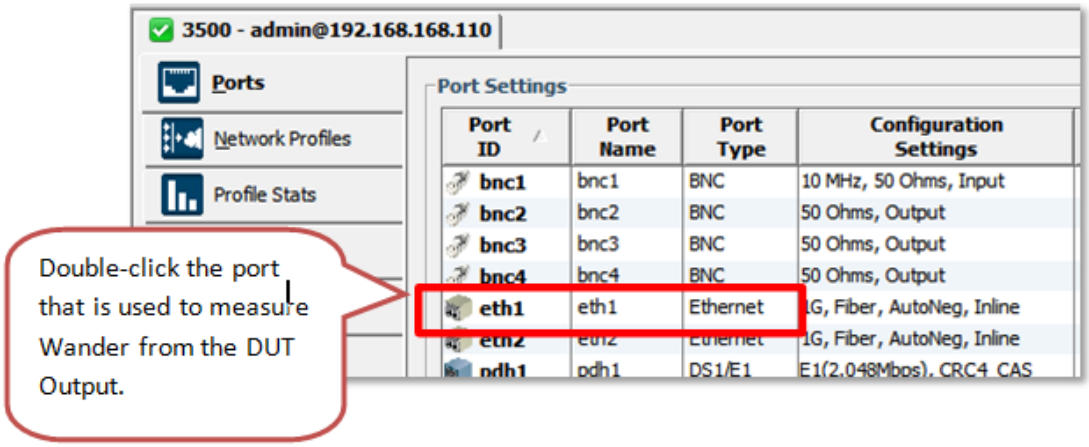
The measurement of generated wander MTIE and TDEV is performed by the Anue 3500, and evaluation against the limits specified in ITU-T G.8262 is automatically performed and pass/fail indication is provided by the Anue 3500 GUI.

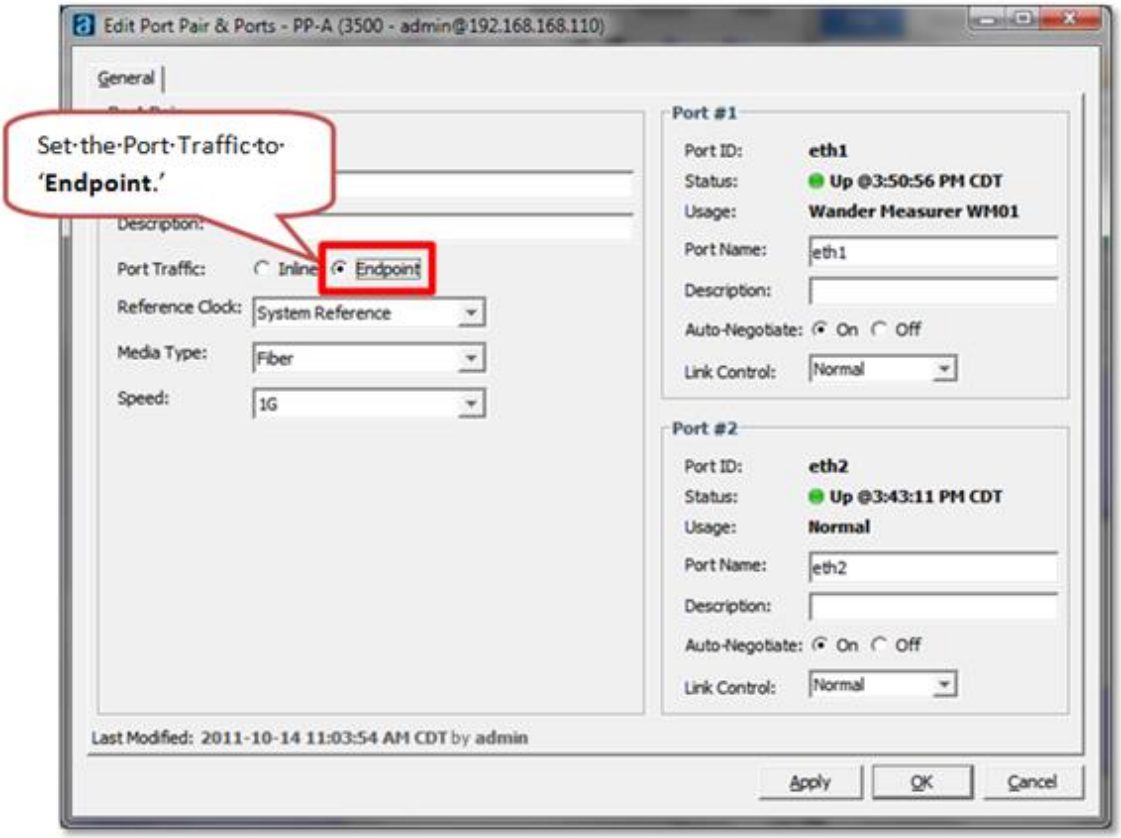
For additional details, see ITU-T G.8262, section 8 *Noise generation*.

Setup

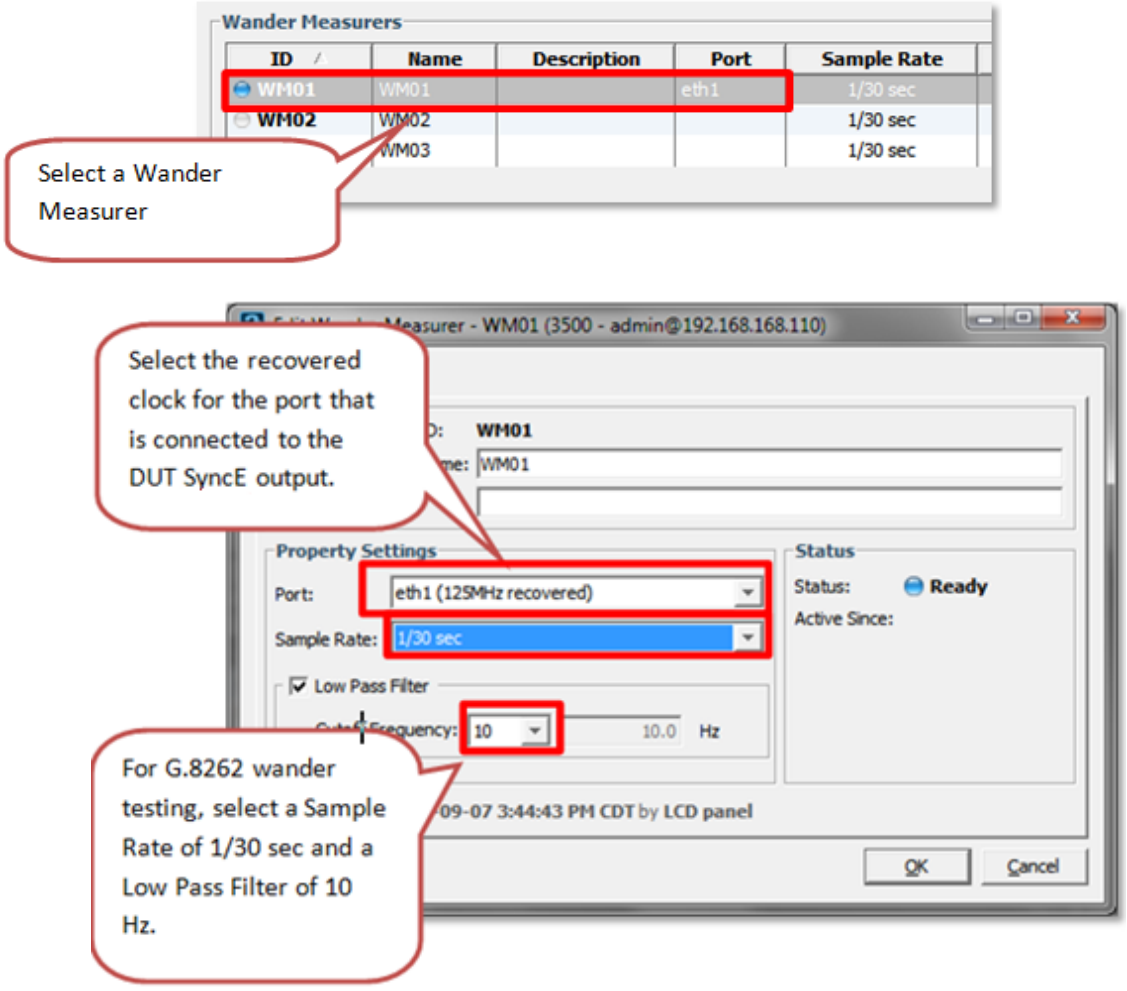

Reference Clock
2.048MHz / 10MHz
/ T1 / E1
Ixia Anue 3500
Reference Clock
supplied to DUT –
T1/E1, 2.048MHz, or
SyncE
SyncE
EEC
100M/1G/10G Ethernet
DUT SyncE Output
includes DUT-
generated Wander

1. Connect and configure the Reference Clock Source.
2. Connect the DUT system Ethernet output to the Anue 3500 Ethernet port 1 (eth1) , and configure by using the Anue 3500 Control Panel Ports tab. Double-click the port that will be connected to the DUT EEC Master's Ethernet port. This brings up the **Ethernet Port Property** dialog box.





3. From the Anue 3500 Control Panel Wander tab, configure the Anue 3500 for wander measurement by double-clicking a Wander Measurer. This brings up the **Edit Wander Measurer** dialog box.



Step-by-Step Instructions

1. The test begins when the configuration is complete.

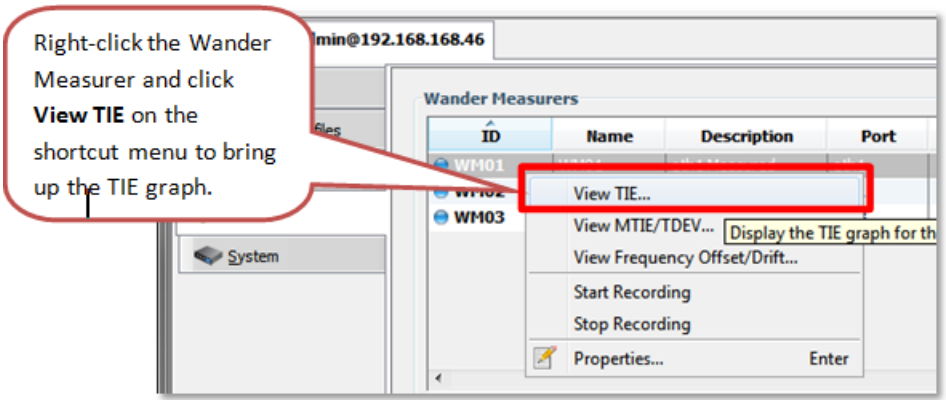
Test Variables

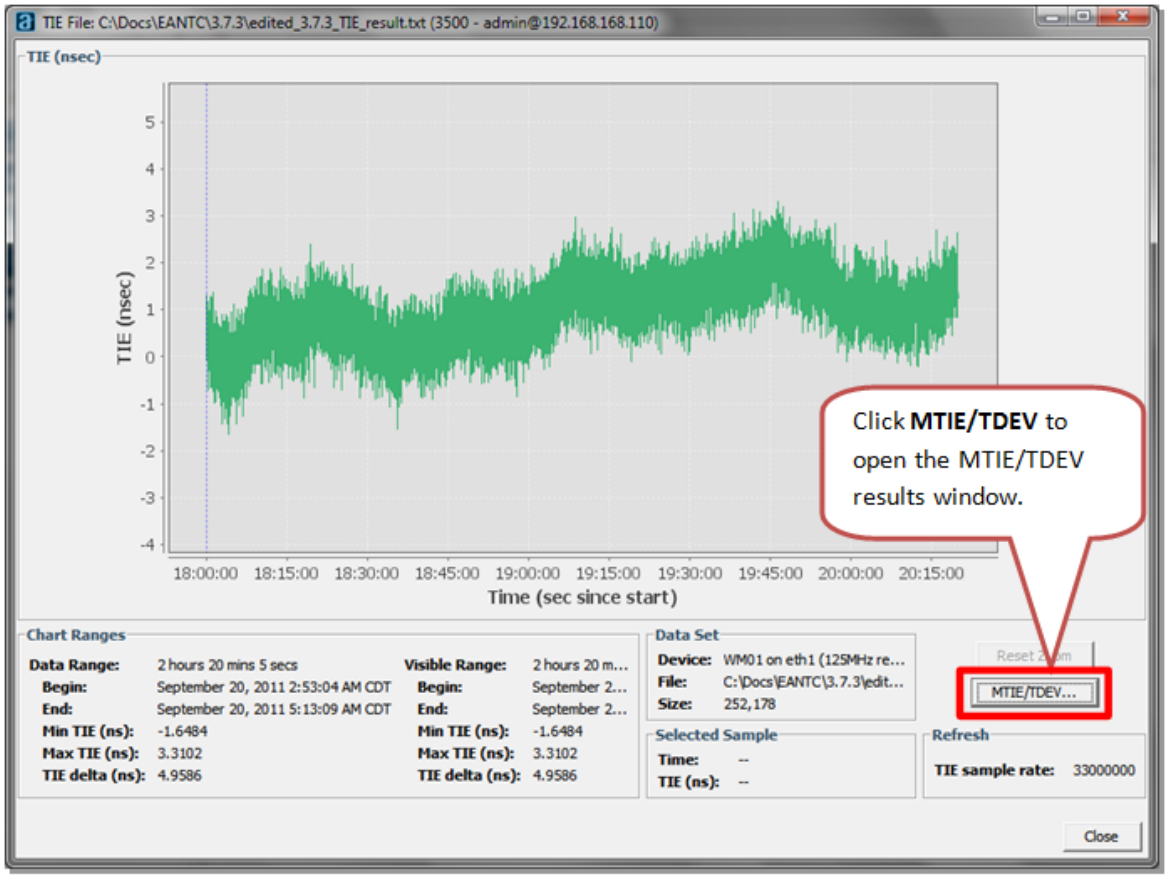
Repeat the test with the following variations:

- Test multiple Ethernet speeds and on all supported interfaces (10G, 1G, and copper/optical).

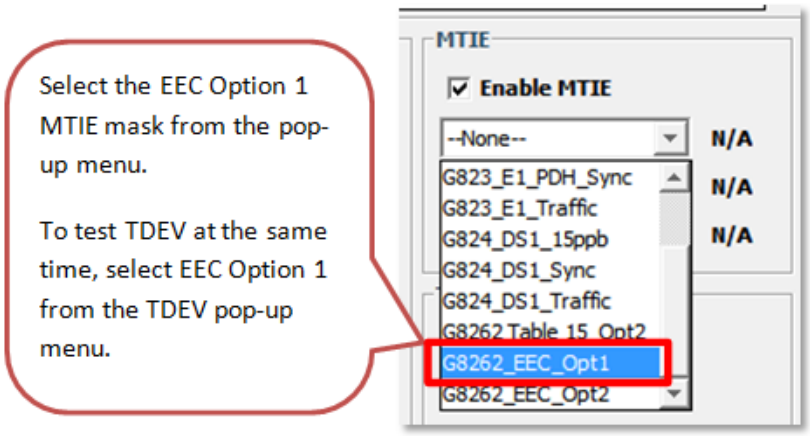
Results Analysis

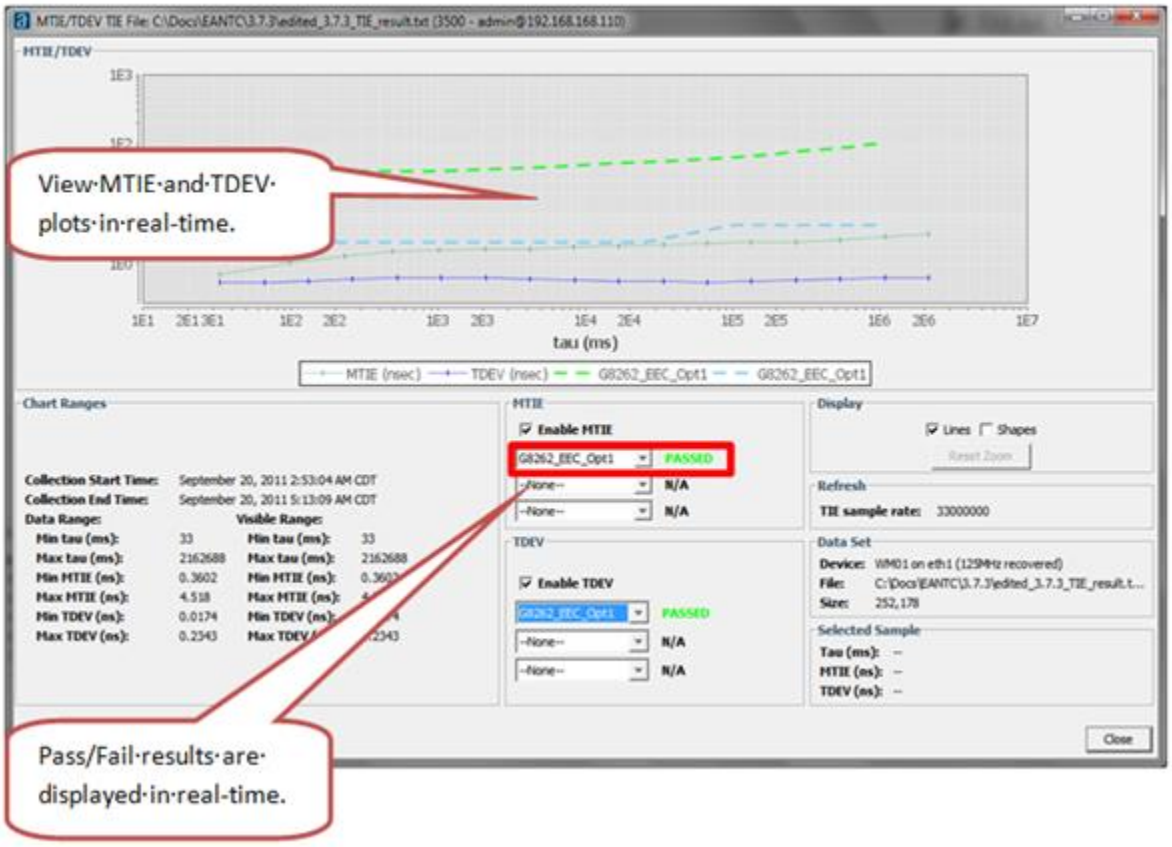
1. From the Anue 3500 Control Panel Wander tab, open the TIE graph and MTIE/TDEV results graphs.





2. Evaluate G.8262 Option 1 by configuring the masks in the MTIE/TDEV Results Graph.





3. According to G.8262 Section 8, the measurement interval for TDEV measurement is 12 times tau, with a maximum tau of 1,000 seconds. Allow results to accumulate for 3h20m (12,000 seconds) for a G.8262 compliant TDEV test result.
4. For MTIE results, the test should be conducted until the maximum tau value present in the selected mask has a measurement value.
5. Evaluate G.8262 Option 2 by selecting the Option 2 masks as in Step 2-3. The Option 1 and Option 2 results can be collected at the same time and shown on the same graph. Pass/Fail evaluation for both masks appear in real-time.
6. The Anue 3500 provides automatic and real-time pass/fail results in the MTIE/TDEV graph window, both in graphical MTIE and TDEV format as well as simple pass and fail indication. Results appear for up to three MTIE masks and three TDEV masks at the same time.
7. When you close the TIE window, you are prompted to save the TIE data to a file. You can save the data for later analysis.

Conclusions

ITU-T G.8262 provides requirements for testing noise generation for Synchronous Ethernet clocks. These tests must be completed for Synchronous Ethernet equipment.

Test Case: Wander Tolerance

Overview

The EEC is required to tolerate certain input wander conditions without causing a failure of operation of the device. ITU-T G.8262 provides test parameters to evaluate the tolerance of an EEC to input wander.

Objective

This test measures the DUT's ability to tolerate the maximum level of wander (phase noise) that may be present in the network without causing failure of the synchronization system.

The wander introduced to the DUT (input wander) must not cause any of the following:

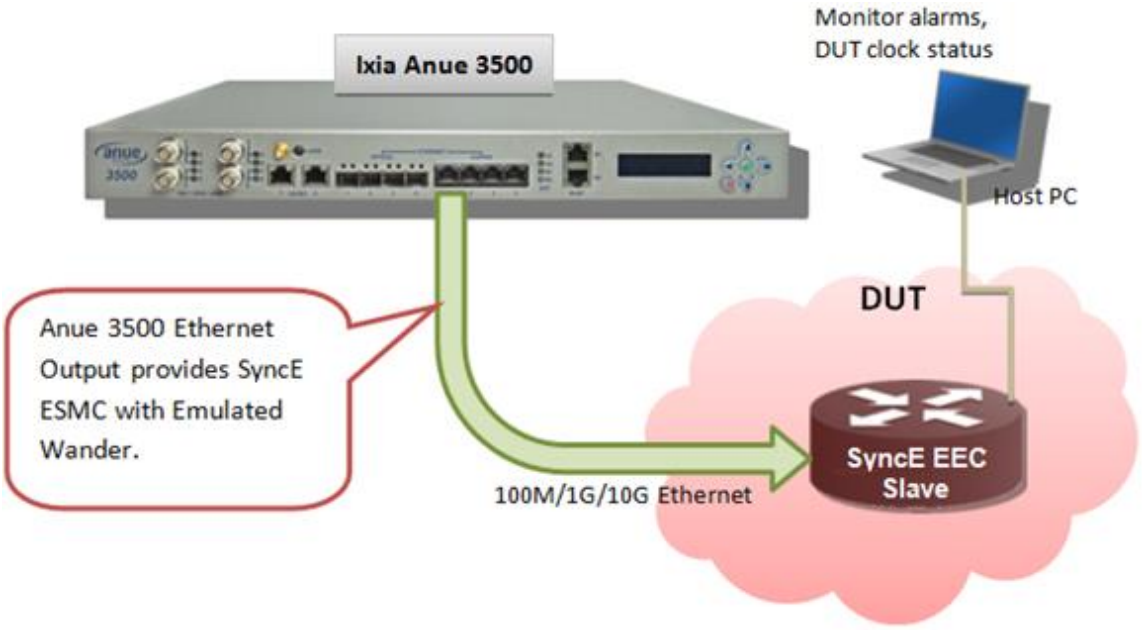
- Alarms
- The clock to switch reference
- The clock to go into holdover

Input wander is specified in terms of Maximum Time Interval Error (MTIE) and Time Deviation (TDEV).

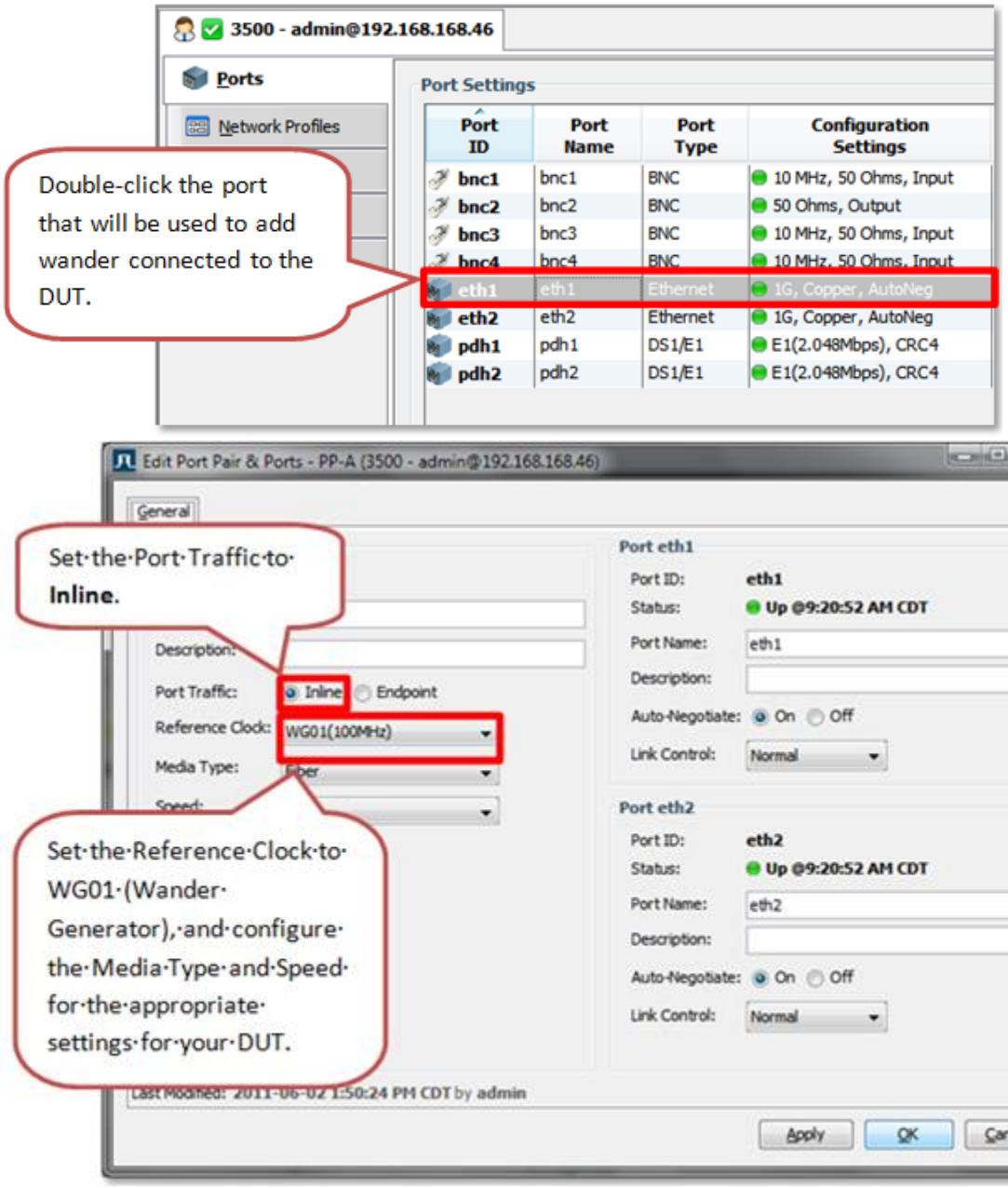
For the wander tolerance test, wander is generated by the Anue 3500. Evaluation of passing and failing is accomplished by observing the DUT alarms and clock status.

For additional details, see ITU-T G.8262, section 9 *Noise tolerance*.

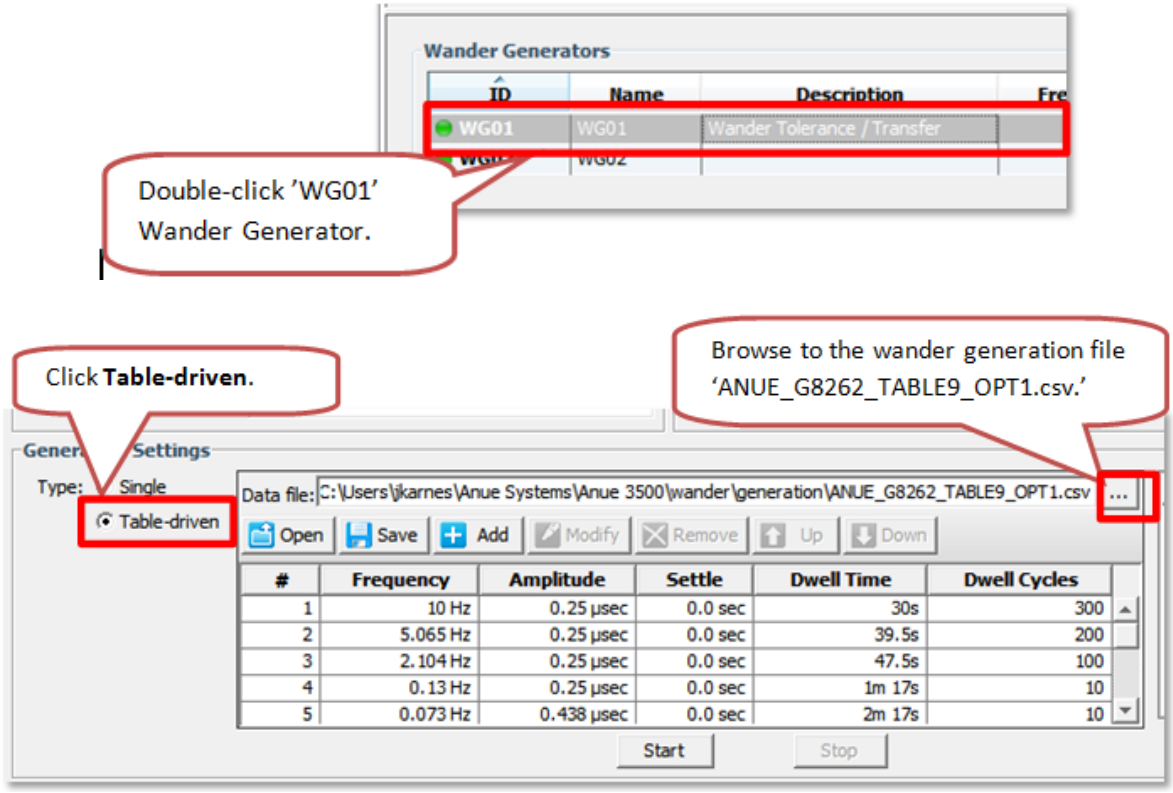
Setup


Monitor alarms,
DUT clock status
Ixia Anue 3500
Host PC
DUT
Anue 3500 Ethernet
Output provides SyncE
ESMC with Emulated
Wander.
100M/1G/10G Ethernet
SyncE EEC
Slave

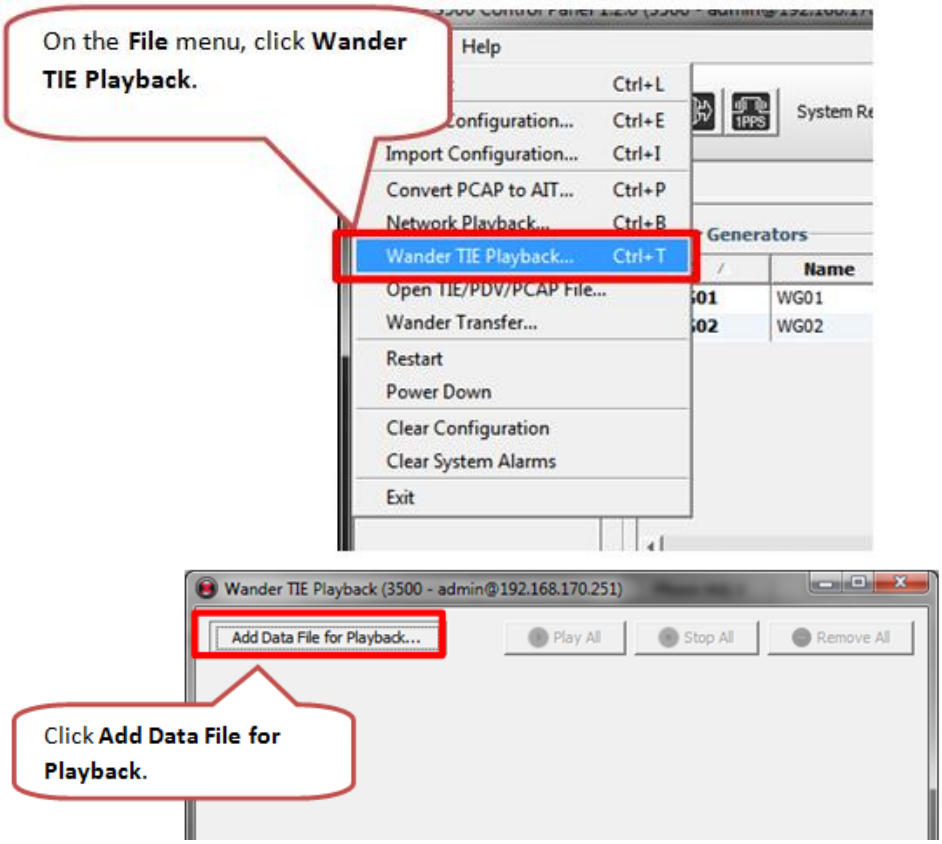
1. Connect the DUT EEC Slave's Ethernet input (100M/1G/10G) to an Anue 3500 Ethernet port (Optical or Copper, as needed), and configure by double-clicking the selected port in the Anue 3500 Control Panel Ports tab.

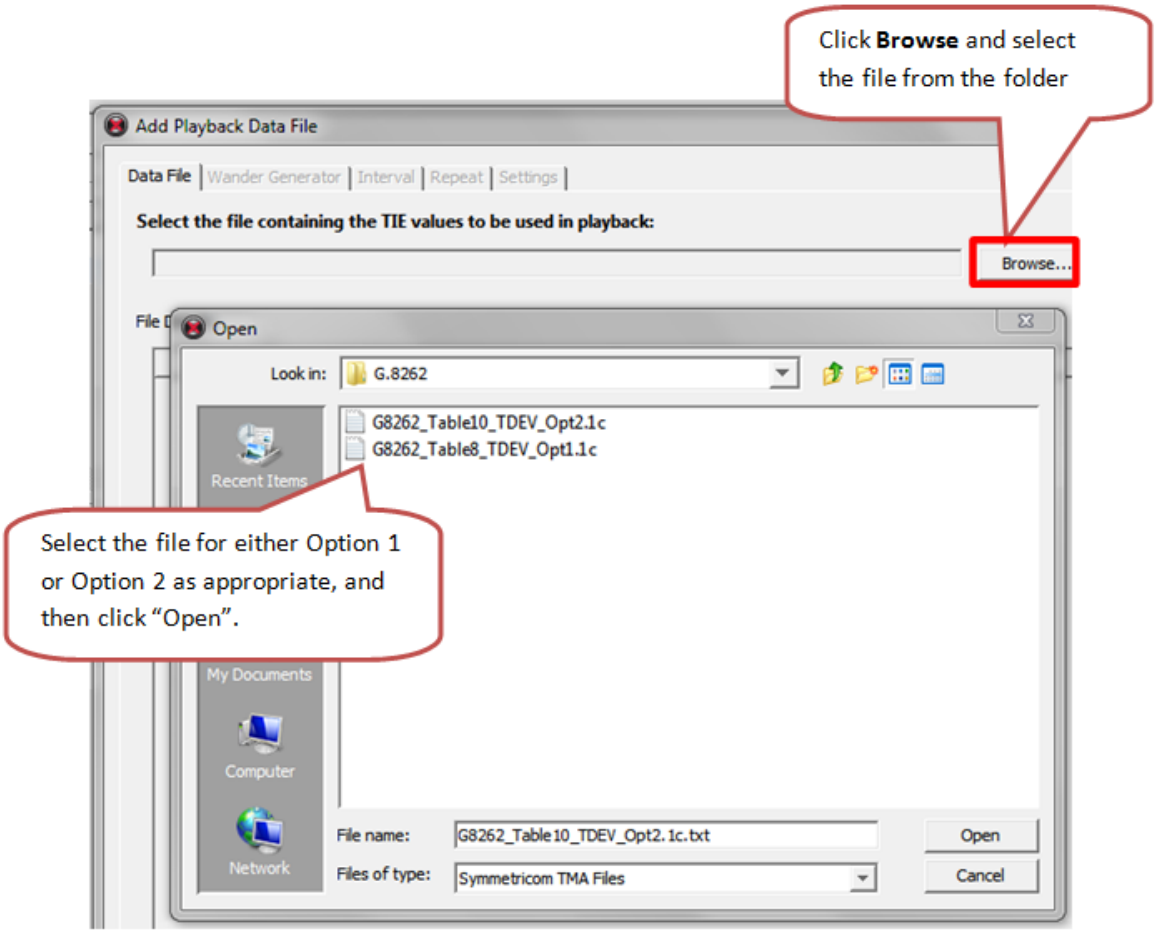


2. Configure wander generation to add the specified wander with the Anue 3500 Control Panel.
    a. For EEC-Option 1, you can use Sinusoidal wander. Configure by using the Ixia Anue 3500 Control Panel Wander tab.



b. For EEC-Option 1 or EEC-Option 2, you may use the TDEV noise generation. Configure by using the Ixia Anue 3500 Control Panel ‘TIE Playback’ feature.

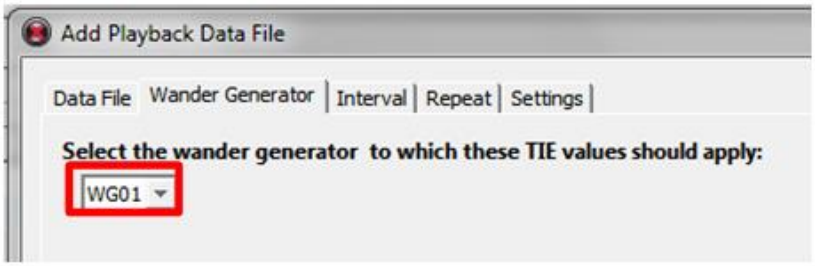




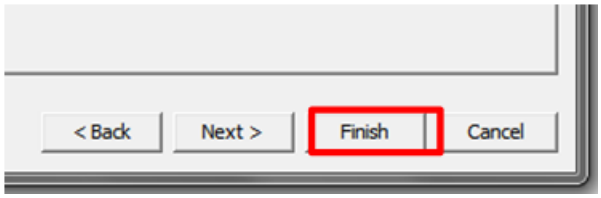
Note: the TDEV noise files are located in the following folder, by default:

%USERPROFILE%"\Anue Systems\Anue 3500\inputnoisefiles\G.8262"

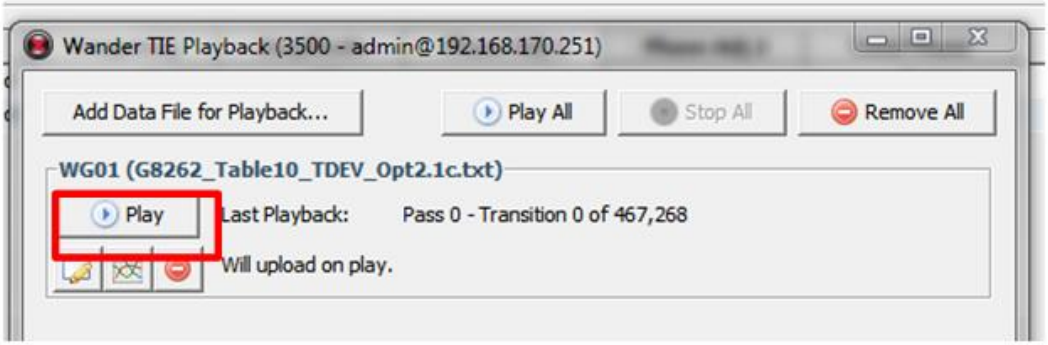
c. Select a Wander Generator:



d. Next, click **Finish**.



e. To begin the test, click **Play**.



3. To make the 3500 emulate the EEC Master, set up ESMC Generation on the Ethernet port with the Anue 3500 Control Panel Ports tab.

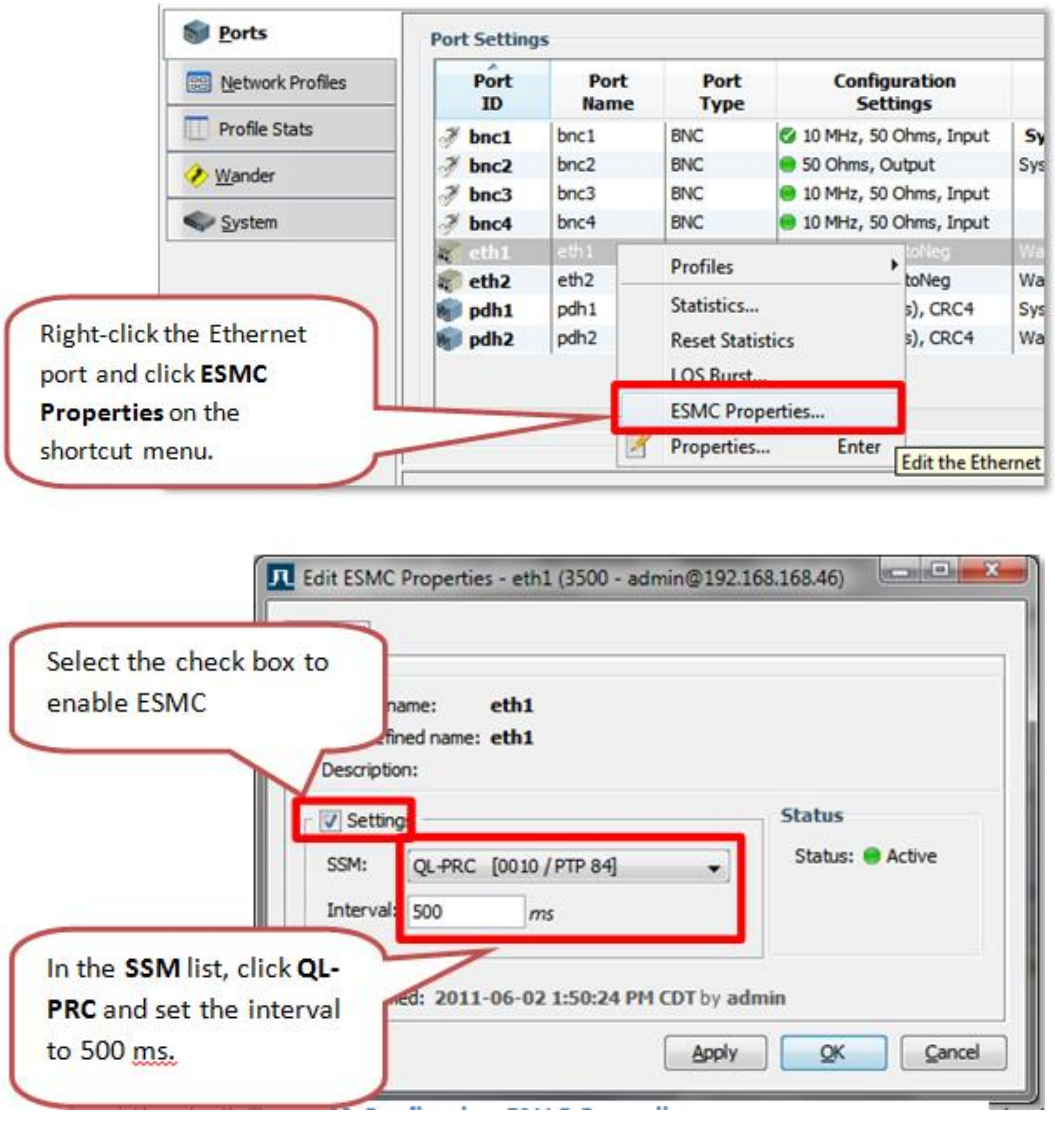
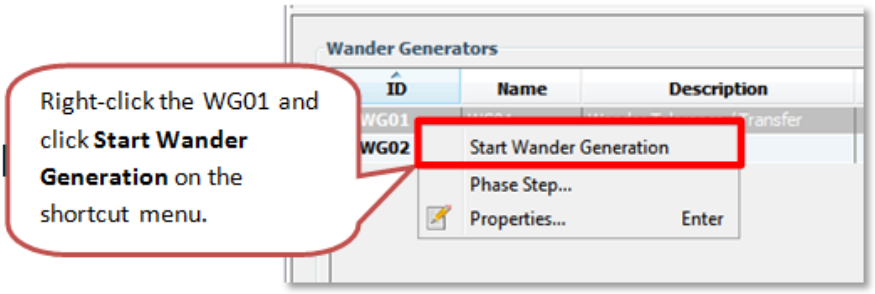


Figure 3 Configuring ESMC Properties

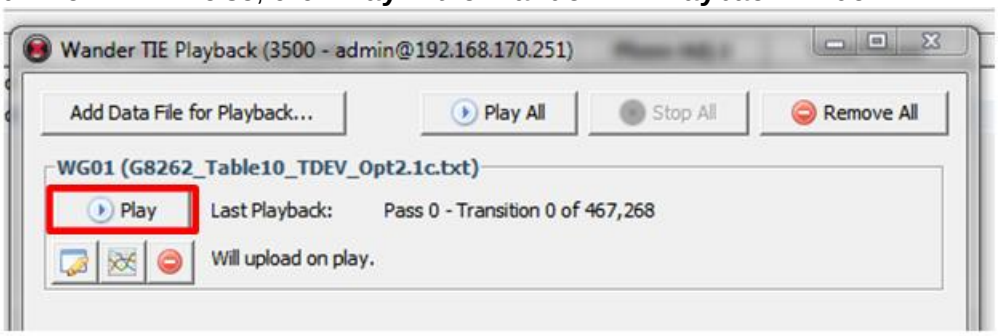
4. Attach the Host PC to the DUT to monitor the clock status and alarms (see DUT documentation) for the duration of the test.

Step-by-Step Instructions

1. Start the test, and begin generating wander.
    a. For sinusoidal wander, start the WG01 Wander Generator in the Wander tab of the Anue 3500 GUI.



    b. For TDEV noise, click **Play** in the **Wander TIE Playback** window.



2. During the duration of the wander generation, monitor the DUT until the wander generation is complete. For sinusoidal wander, this is until the table has been completed. For TDEV noise, monitor until the file has completed at least one playback cycle. Note that this is several hours in either case and it varies depending on configuration.
   Note any occurrence of the following:
   - Alarms
   - Clock switch reference
   - Clock going into holdover

Test Variables

Repeat the test with the following variations:

- Test multiple Ethernet speeds and on all supported interfaces (10G, 1G, and copper/optical)

Results Analysis

The test fails of there is any occurrence of the following while monitoring the DUT:

- Alarms
- Clock switch reference
- Clock going into holdover

Conclusions

ITU-T G.8262 provides requirements for testing noise tolerance for Synchronous Ethernet clocks. These tests must be completed for Synchronous Ethernet equipment.

Test Case: Wander Transfer

Overview

An EEC is required to operate as a low-pass filter with respect to transfer of wander on the synchronization interface to the downstream EEC clocks connected to its master ports, with minimal additional wander to be added. ITU-T G.8262 specifies tests to measure the wander transfer performance of the EEC.

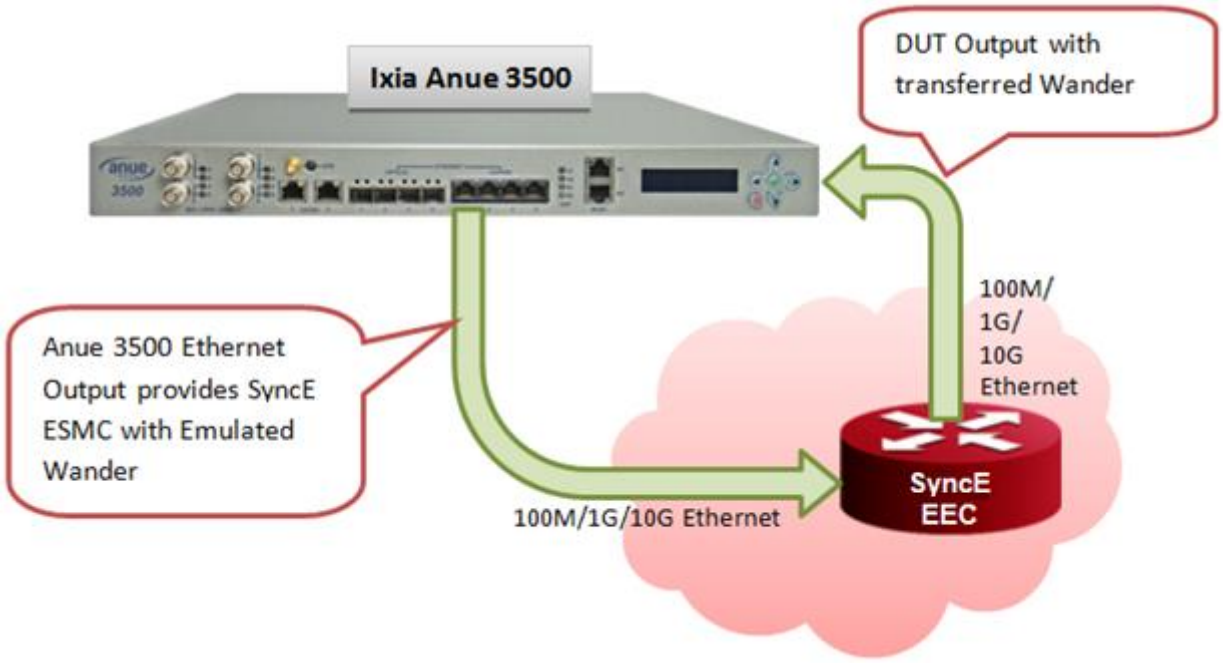
Objective

This test measures the amount of SyncE wander introduced to the DUT (input wander) that is transferred to the output of the DUT, in terms of gain and bandwidth. The DUT normally is expected to track the master clock within a specified pass band, while filtering higher-frequency noise and not generating additional noise within the pass band.

For the wander transfer test, input wander is generated on one port of the Anue 3500. The output wander from the DUT is measured on another port of the Anue 3500.

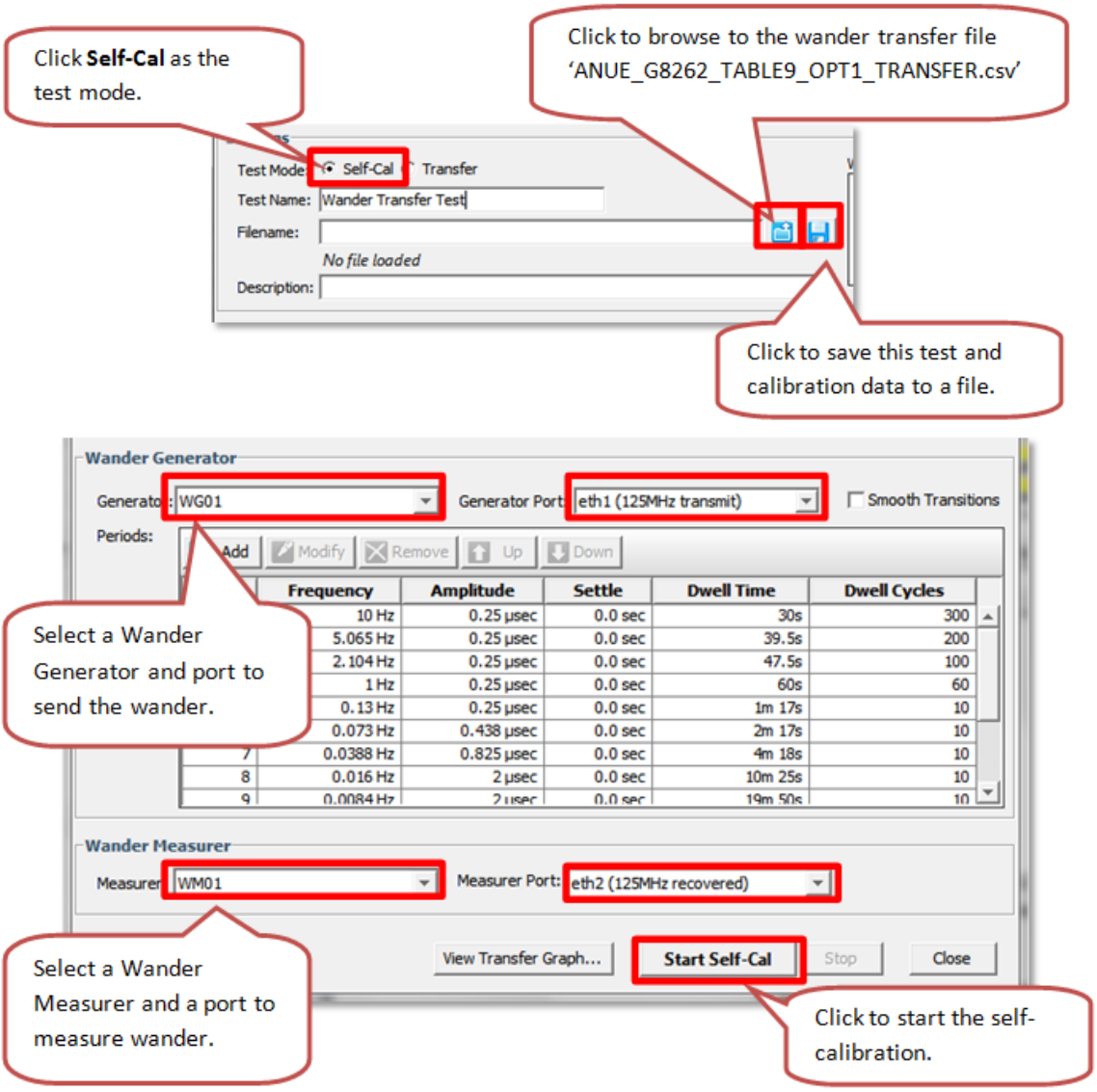
For additional details, see ITU-T G.8262, section 10 *Noise transfer*.

Setup



1. For 10.1 EEC-Option 1 Testing, use the Wander Transfer tool in the Ixia Anue 3500 Control Panel.

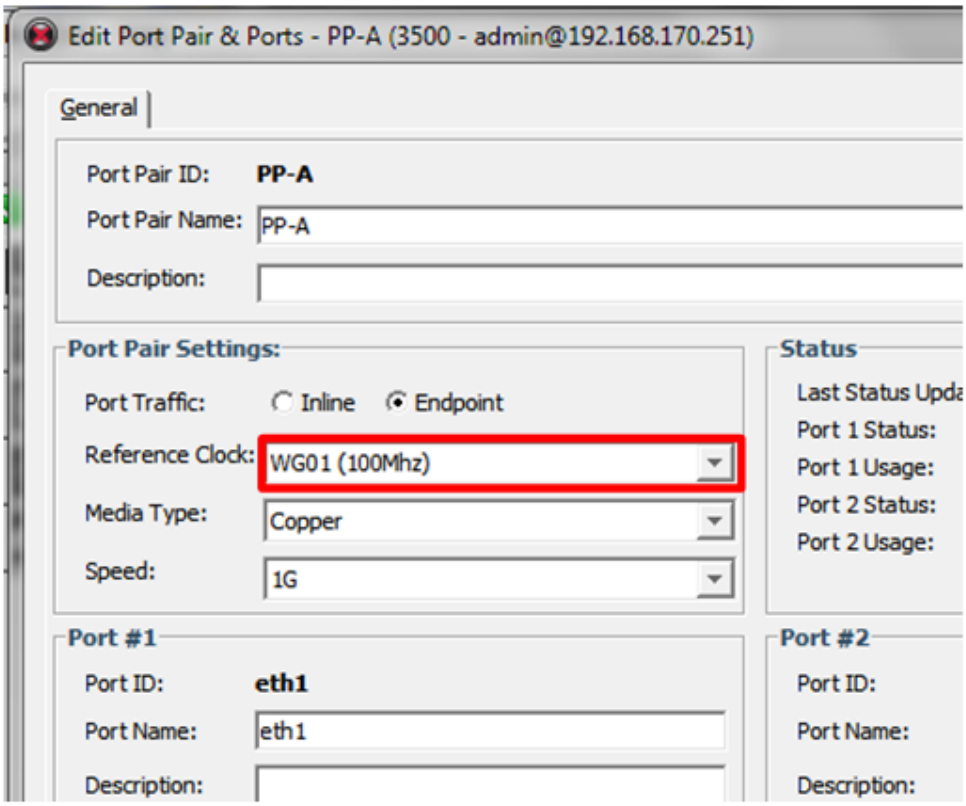
a. From the Anue 3500 Control Panel, on the **File** menu, click **Wander Transfer** to enter Wander Transfer mode.
b. First, calibrate the 3500 for wander transfer by connecting an Ethernet cable between the two Ethernet test ports (eth1 and eth2), and perform the calibration procedure in steps 3-4 below. *Note: The calibration steps only must be completed one time, and they are optional. To begin testing without calibrating, skip to step 5.*
c. Load the Wander Transfer table and complete the Self-Cal.



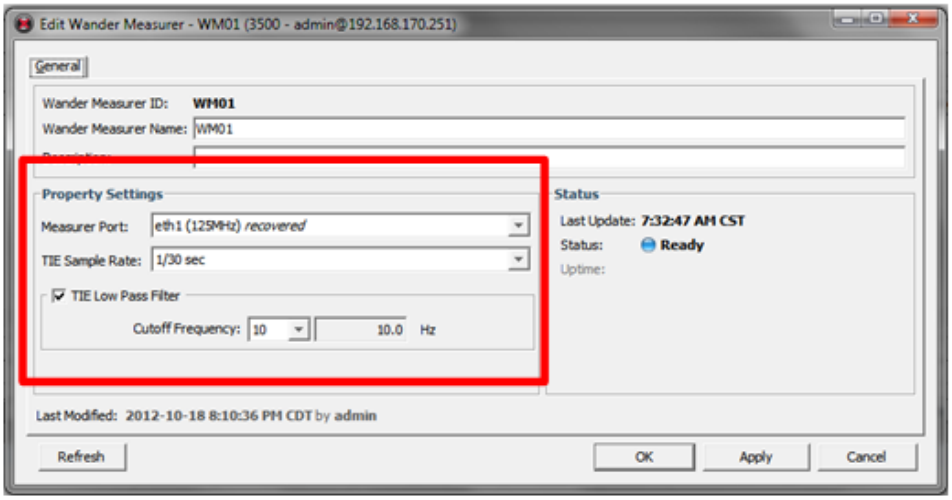
d. Confirm when prompted and the self-calibration begins. Wait for the Self-Cal to complete, and then continue to Wander Transfer testing. We recommend you to save the test file after the calibration completes.
***Note**: For the most accurate measurements, Self-Cal should be completed for each system for all frequencies being measured and for each interface type (Copper or Optical) at least one time for a given test. Subsequent runs of the*

same test can be done with the same calibration data set. Self-Cal can take several hours to run.

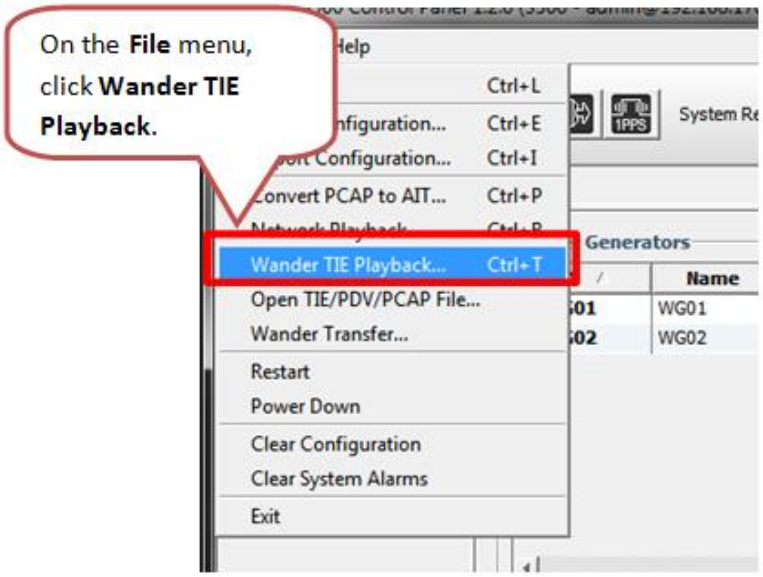
2. For 10.2 EEC-Option 2, test by using the **Wander TIE Playback** and a wander measurer with TDEV mask analysis.
    a. First, configure eth2's clock source to use the wander generator WG01 by double-clicking the port **eth2** in the Ixia Anue 3500 Control Panel **Ports** view.

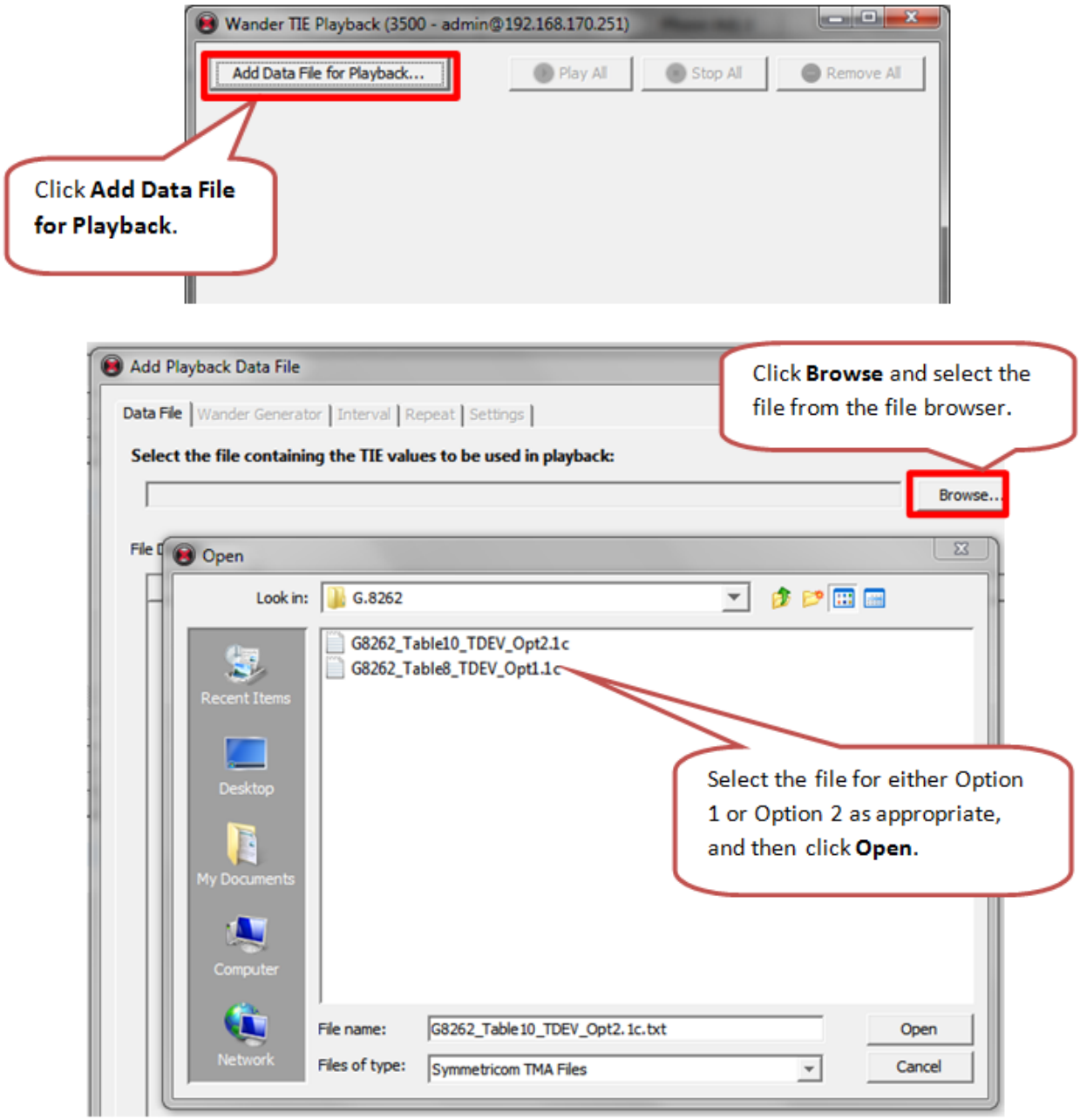


b. Configure a Wander Measurer to measure the recovered clock port **eth1** by using the Ixia Anue 3500 Control Panel **Wander** view. In addition, leave the default settings for 10Hz low-pass filter and also 1/30 second sample rate.



c. Configure wander generation by using the Ixia Anue 3500 Control Panel 'TIE Playback' feature.

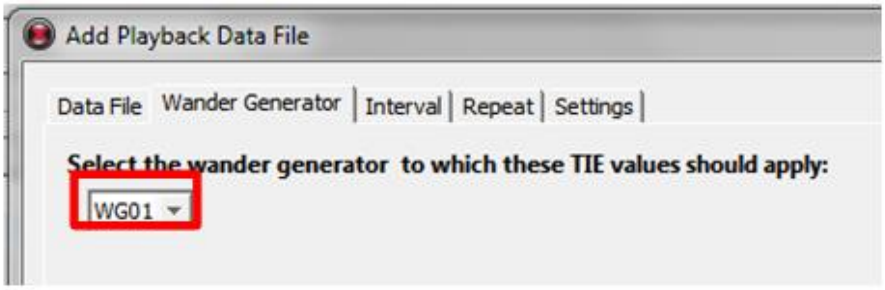




Note: The TDEV noise files are located in the following folder, by default:

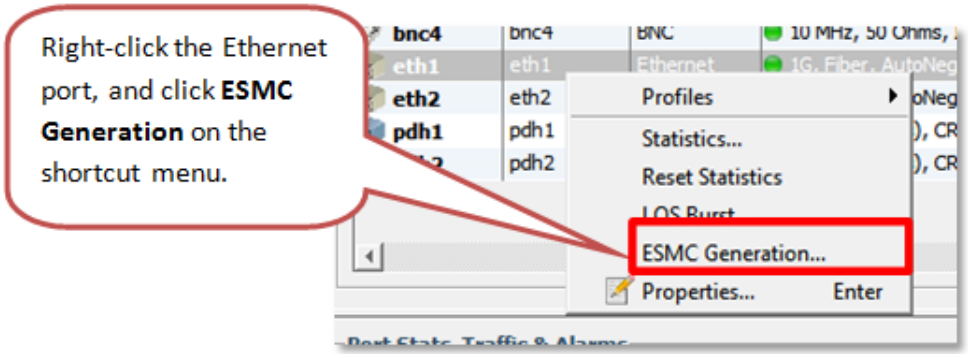
%USERPROFILE%"\Anue Systems\Anue 3500\inputnoisefiles\G.8262"

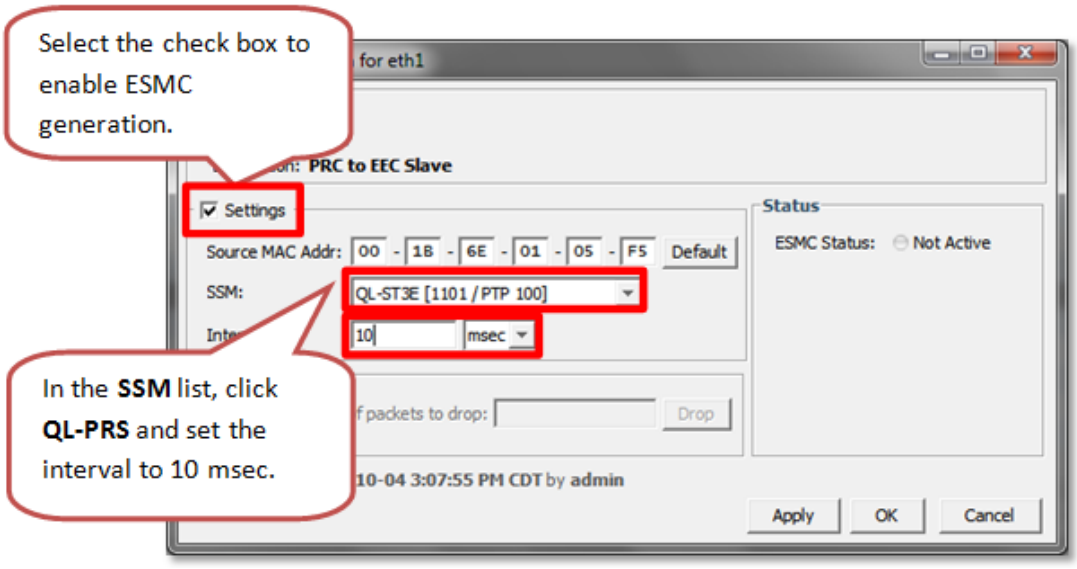
d. Select a Wander Generator:



e. Next, click **Finish**.

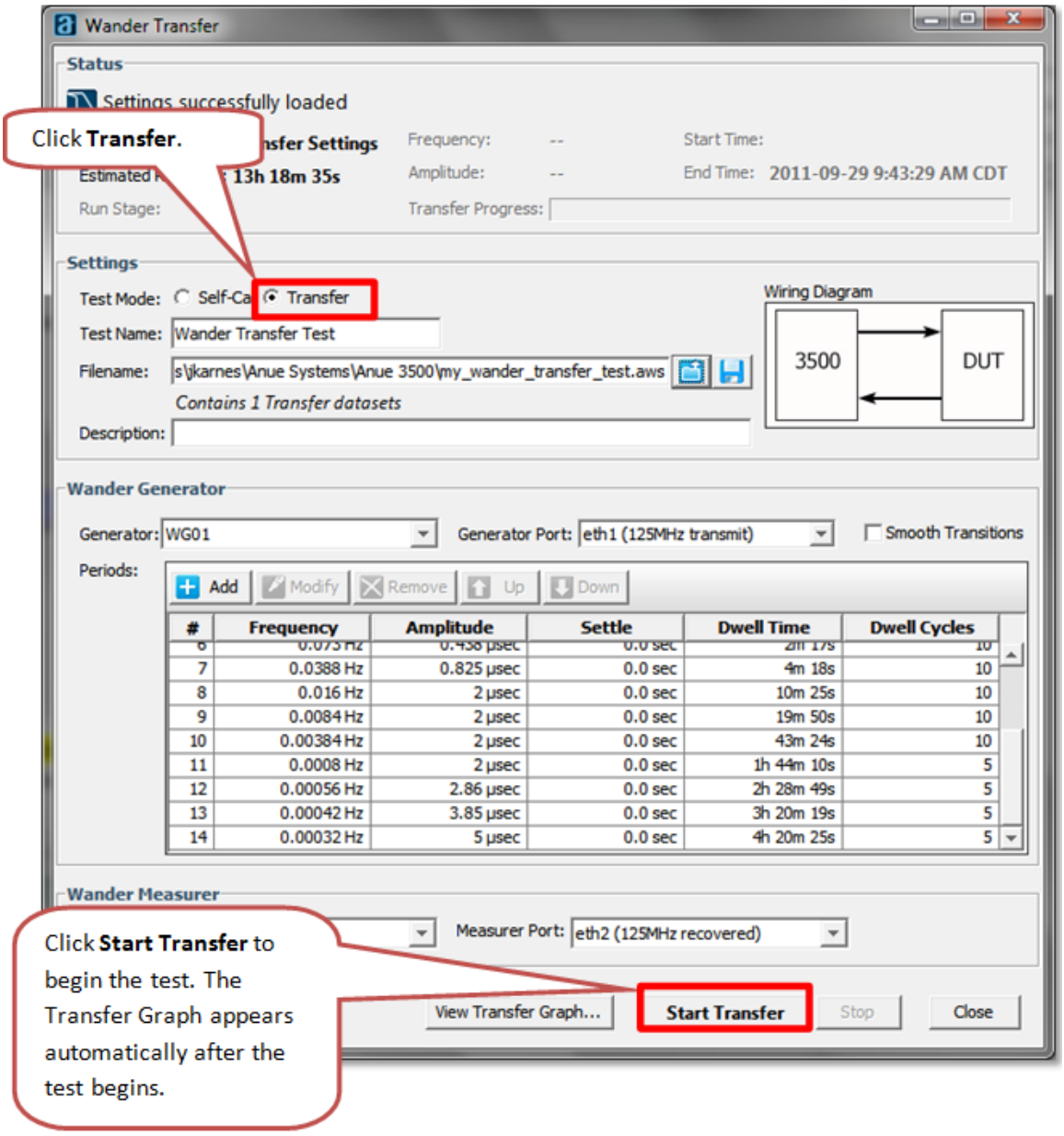
3. Connect each of the 3500's Ethernet ports to the DUT Ethernet ports (100M/1G/10G) as shown in the Test Setup diagram.
4. To make the 3500 emulate the EEC Master, set up ESMC Generation on the Ethernet port with the Anue 3500 Control Panel Ports tab.



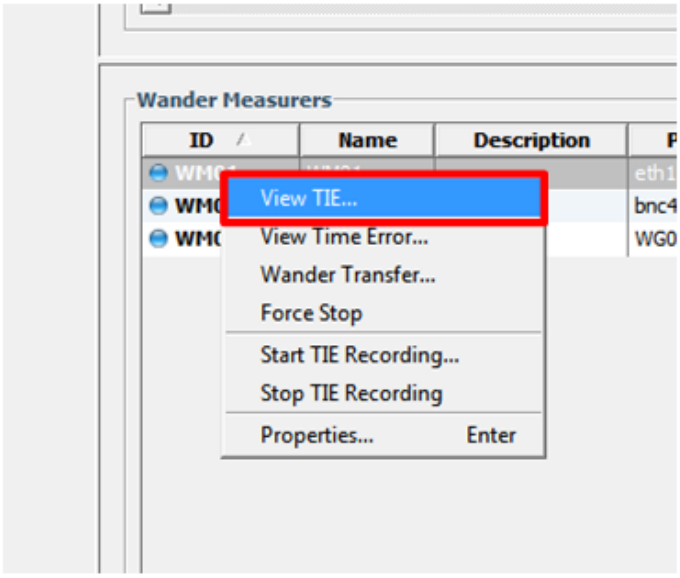


Step-by-Step Instructions

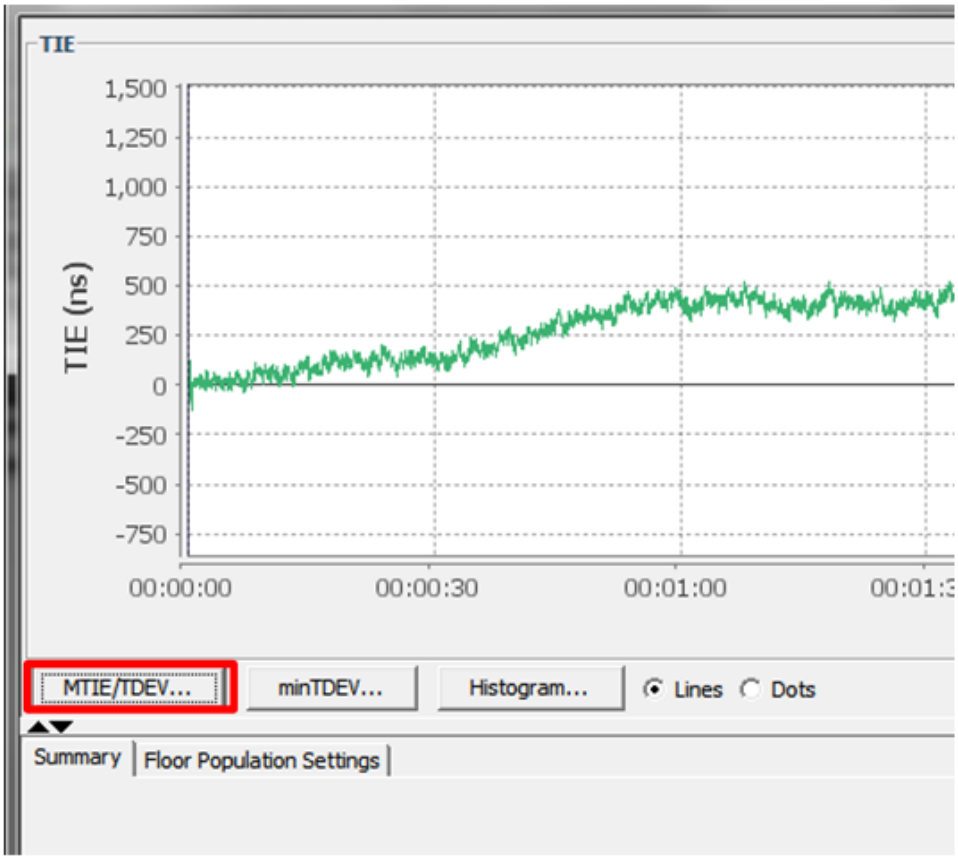
1. For EEC-Option 1 with Sinusoidal Wander, start the Wander Transfer test.



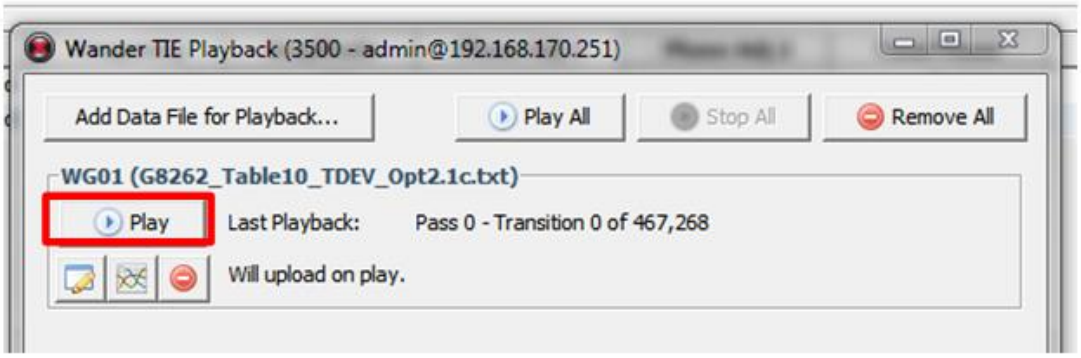
2. For EEC-Option 2, begin the wander measurer and also start the TIE Playback of the TDEV noise file.
    a. First, start the wander measurer by right-clicking the wander measurer in the Wander view, and then clicking **View TIE**.



Click **MTIE/TDEV** to view MTIE and TDEV graphs.



    b. Next, click **Play** in the **Wander TIE Playback** window to start noise playback.



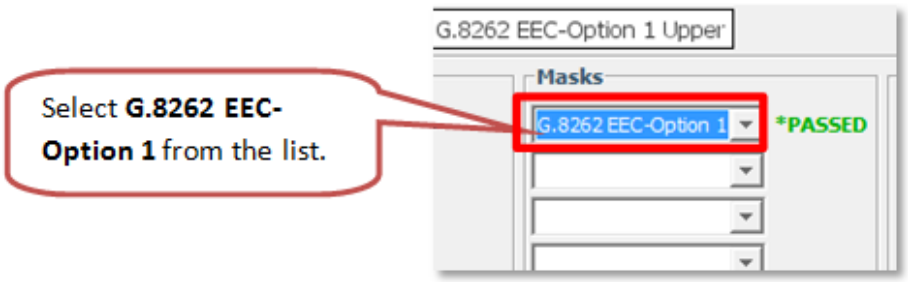
Test Variables

Repeat the test with the following variations:

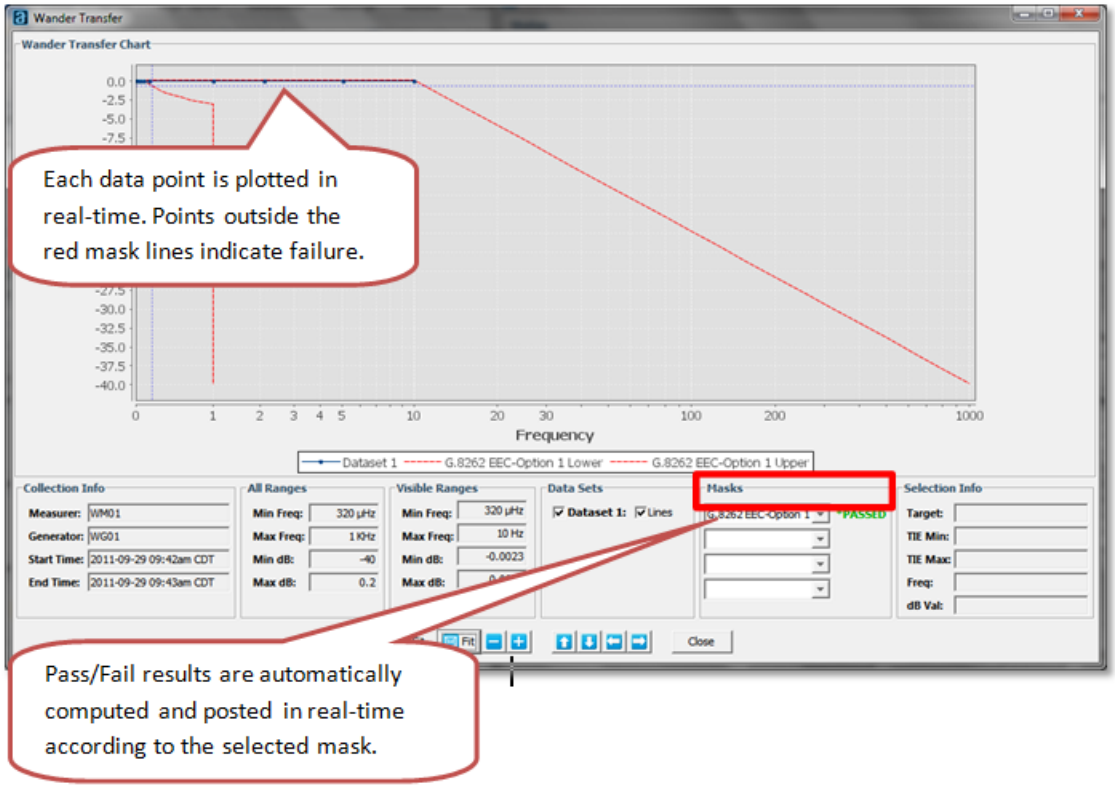
- Test multiple Ethernet speeds and on all supported interfaces (10G, 1G, and copper/optical).
- Test with both EEC-Option 1 (sinusoidal wander transfer) and also EEC-Option 2 (TDEV wander transfer).

Results Analysis

1. Analyze EEC-Option 1 results:
    a. As soon as the first step in the Wander Generator table has completed, the Wander Transfer graph appears, showing the results in real-time as each step is completed. You can also open the Wander Transfer graph at any time during the test by clicking **Transfer Graph**.
    b. When the Wander Transfer graph is opened, select the mask 'G.8262 EEC-Option 1' to have the results automatically evaluated based on the mask.



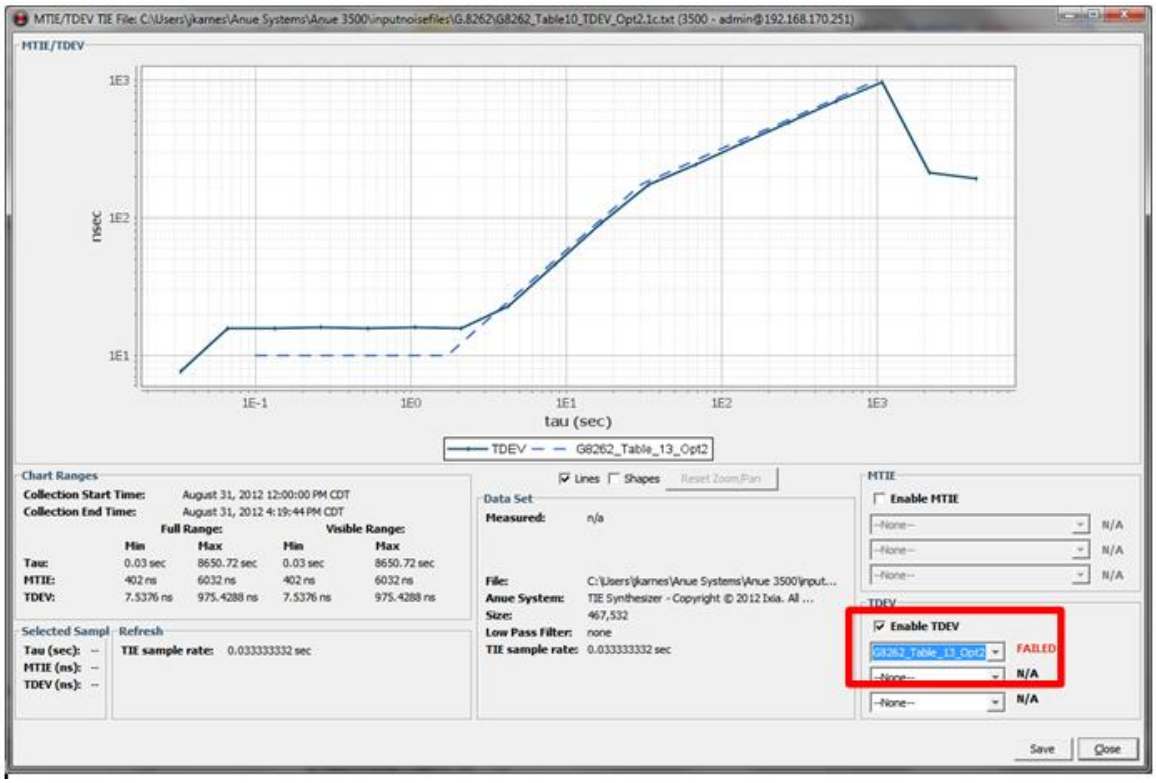
c. The results appear in the Transfer Graph.



d. The Anue 3500 calculates pass/fail results in real-time for the duration of the test, while graphically plotting the data points.

e. After the test completes, you may save the results in the **Wander Transfer** dialog box. Multiple tests can be run and saved to the same file. These multiple data sets can be reviewed concurrently on the same graph.

2. For EEC-Option 2 TDEV wander transfer, evaluate the TDEV noise according to the selected mask. In the **MTIE/TDEV** window, select the **Enable TDEV** check box, and select the mask 'G8262_Table13_Opt2.' Automatic PASS/FAILED result appears in the TDEV window.



Conclusions

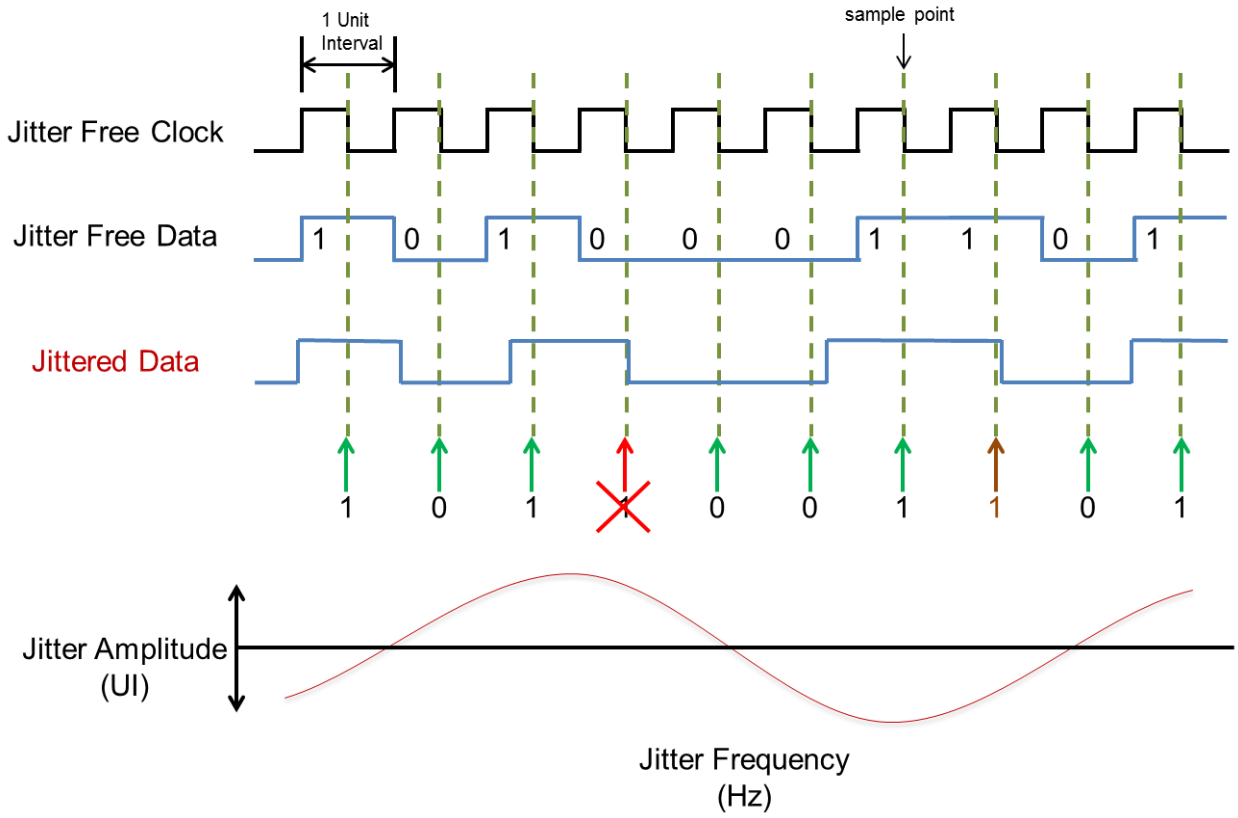
ITU-T G.8262 provides requirements for testing noise transfer for Synchronous Ethernet clocks. These tests must be completed for Synchronous Ethernet equipment.

Test Case: Jitter Compliance

Overview

The term jitter being discussed here refers to the ‘timing jitter’ or ‘physical layer jitter’ present in the SyncE EEC. Whereas wander affects ‘Synchronization Quality’, jitter affects ‘Data integrity’ quality i.e. ‘Bit Errors’, leading to loss of throughput.

Jitter is better explained as the short-term variations of the significant instants of a timing signal from their ideal positions in time (where short-term implies that these variations are of frequency greater than or equal to 10 Hz).



ITU-T G.8262 Section 8.3 specifies the Unit Interval (UI) of the signal for these Ethernet interfaces (supported by ANUE 3500):

- 1G: UI = 0.8ns
- 10G (10GBASE-SR/LR/ER, -LRM): UI = 96.97ps

Note: Copper is currently not supported by the standard and copper is considered not suitable for SyncE applications.

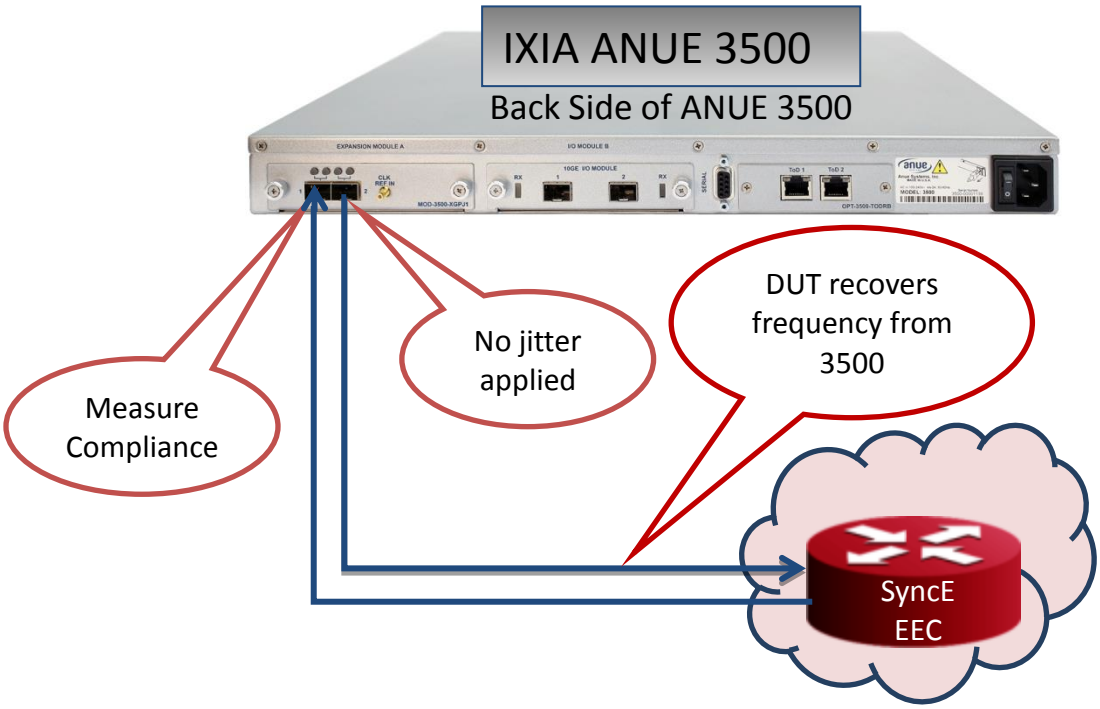
Jitter is measured over a specific frequency range (filtered)

- 1G: 2.5kHz to 10MHz
- 10G: 20kHz to 80Mhz

Objective

Measure the intrinsic jitter at the Synchronous Ethernet output interface in the absence of any input jitter. Measurements should be taken over a 60 second period.

Setup

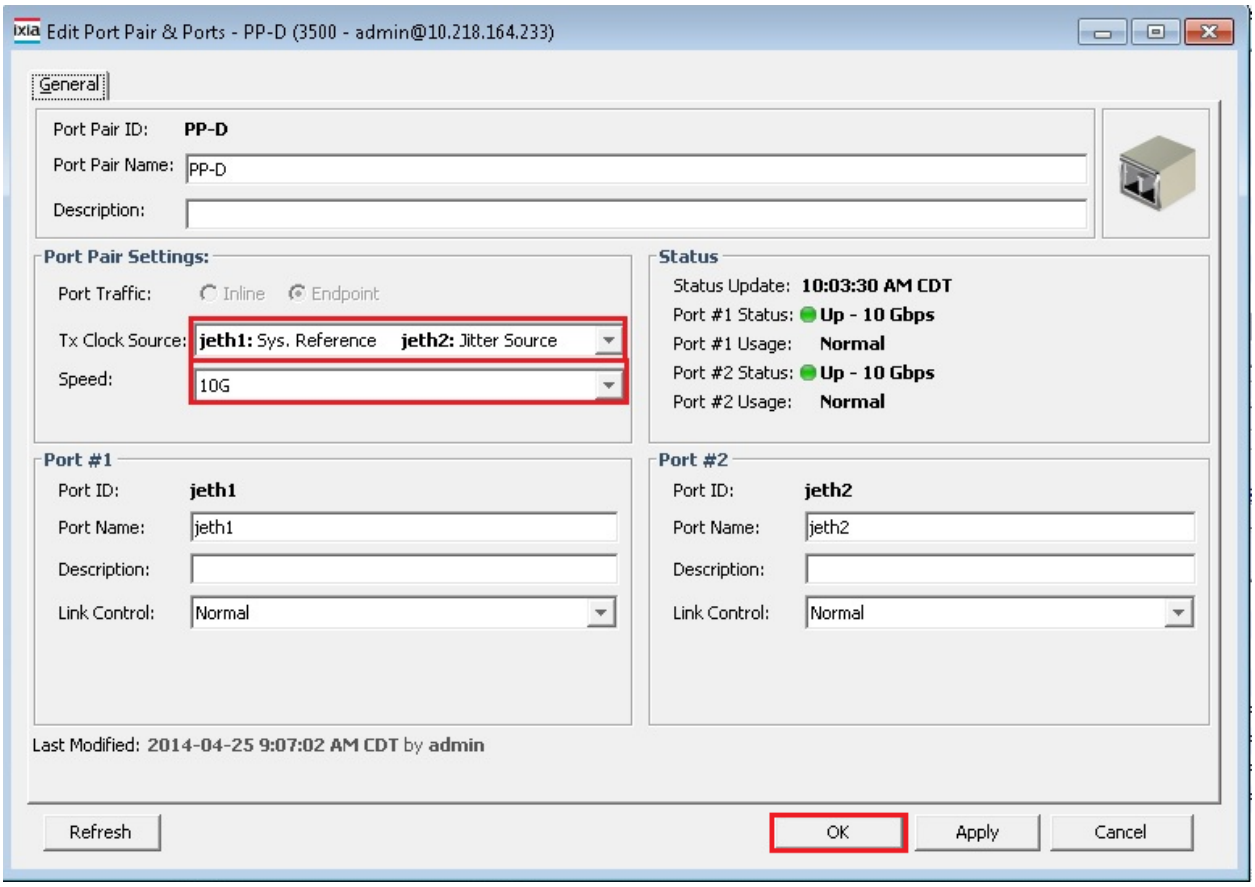


Note: The clock signal going to the DUT is not strictly necessary. For more information, refer to step#3 in ‘Step-by-Step Instructions.’

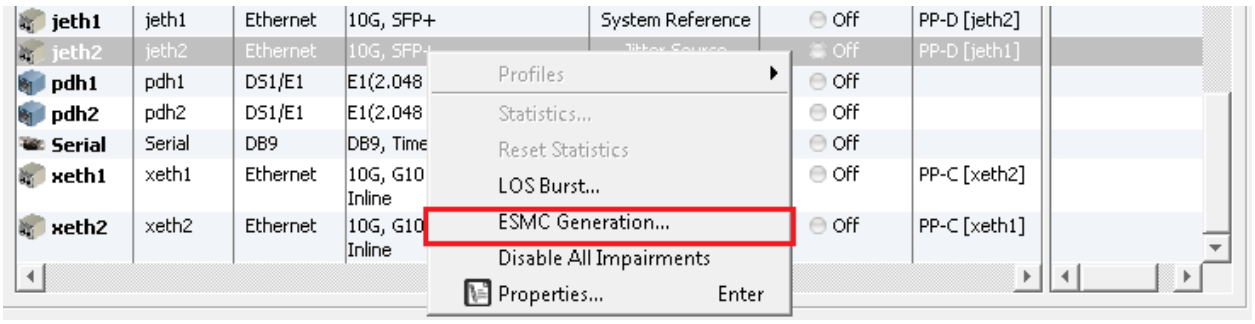
Note: If the customer would like to supply their own timing reference for their DUT, then they are free to do so with the 10 Hz Clock Recovery Bandwidth.

Step-by-Step Instructions

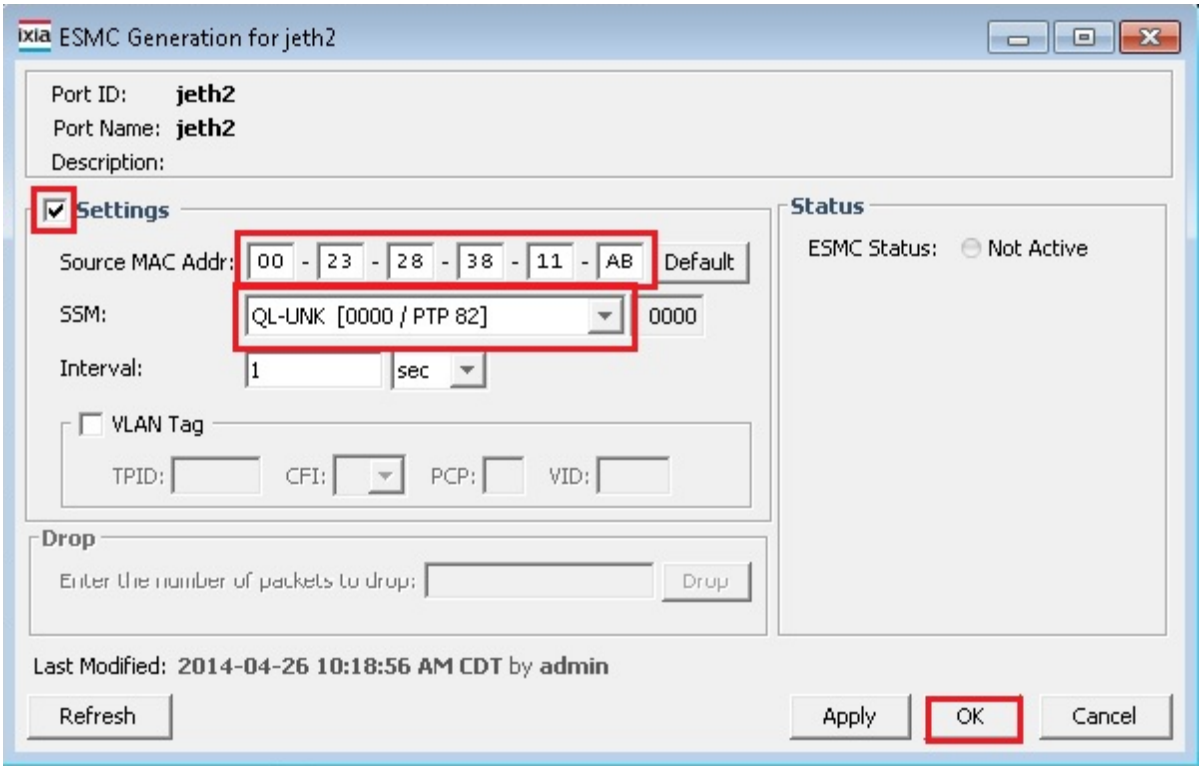
1. Click on ports and select jeth1. Double click to launch ‘Port Properties’ dialog. In the ‘Port Pair Settings’:
    - Set ‘Tx Clock Source’ to “jeth1: Sys Reference jeth2: Jitter Source”
    - Set ‘Speed’ to “10G”
    - Click OK.



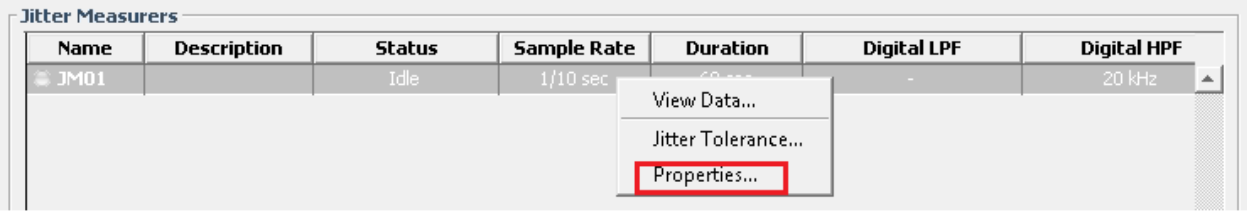
2. Select jeth2 in the ports view and right click.
    - Select ‘ESMC Generation’ from the menu.



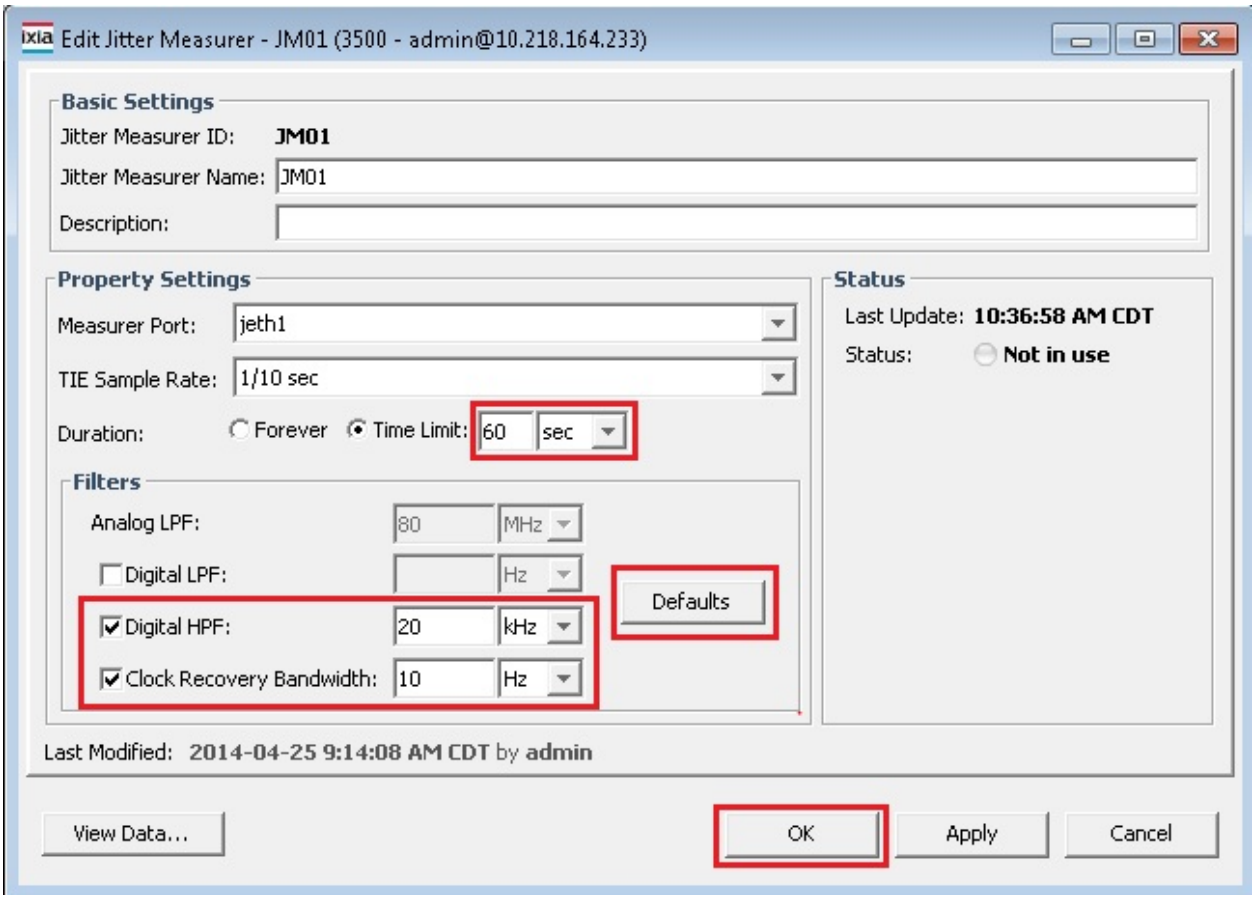
- In the ‘ESMC Generation’ dialog, select the checkbox next to ‘Settings’. Optionally, configure the ‘Source MAC Addr’and ‘SSM’.
- Click OK.



3. Go to ‘jitter’ view and select ‘JM01’ in the ‘Jitter Measurer’ tab.
    - Right click and select ‘Properties...’ from the menu to open the dialog.



- In the ‘Properties’ dialog, set measurement duration to 60 seconds and click on ‘Defaults’ to set default filters for standards-compliant testing.
- Click OK.

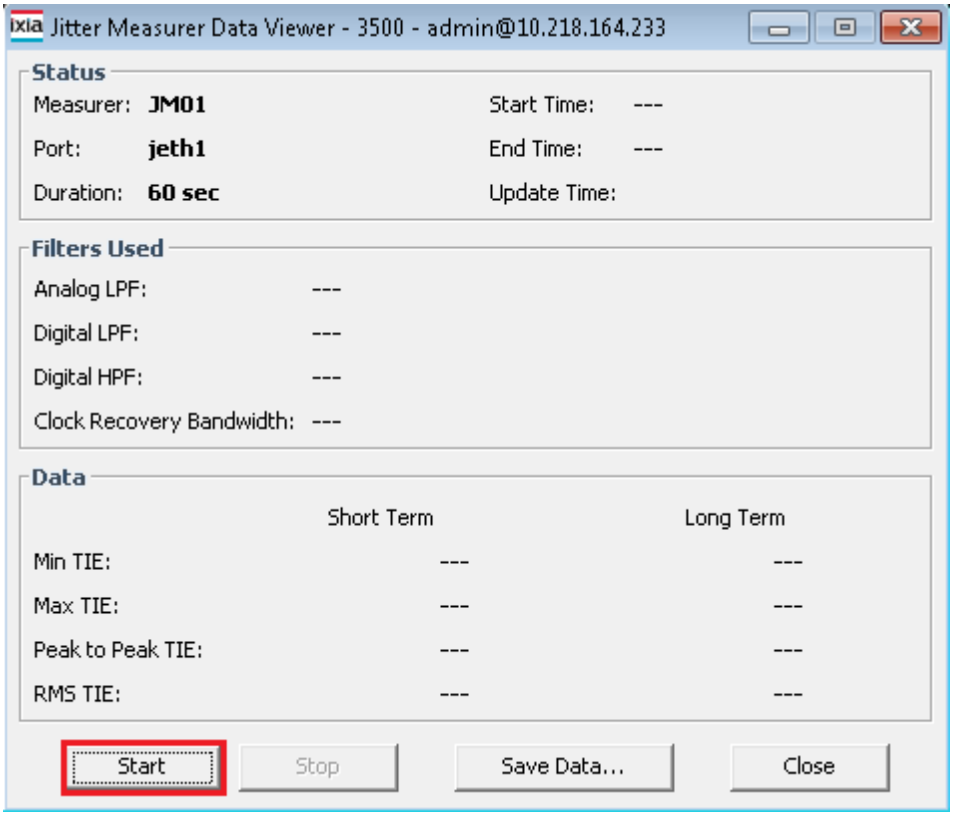


- Optionally, the digital filters can be configured as needed.

  Note: The digital filters are first order with a -20 dB per decade roll-off. The Clock Recovery Bandwidth filter is second order with a -40 dB per decade roll-off.

  Note: The clock signal going to the DUT is not strictly necessary as the function of the 10 Hz Clock Recovery Bandwidth should actually take care of this.

4. Select JM01 again and right click. Select ‘View Data...’ to launch the jitter measurer dialog. Click on ‘Start’.


Jitter Measurer Data Viewer - 3500 - admin@10.218.164.233
Status
Measurer: JM01
Port: jeth1
Duration: 60 sec
Start Time: ---
End Time: ---
Update Time:
Filters Used
Analog LPF: ---
Digital LPF: ---
Digital HPF: ---
Clock Recovery Bandwidth: ---
Data
Short Term
Long Term
Min TIE: --- ---
Max TIE: --- ---
Peak to Peak TIE: --- ---
RMS TIE: --- ---
Start
Stop
Save Data...
Close

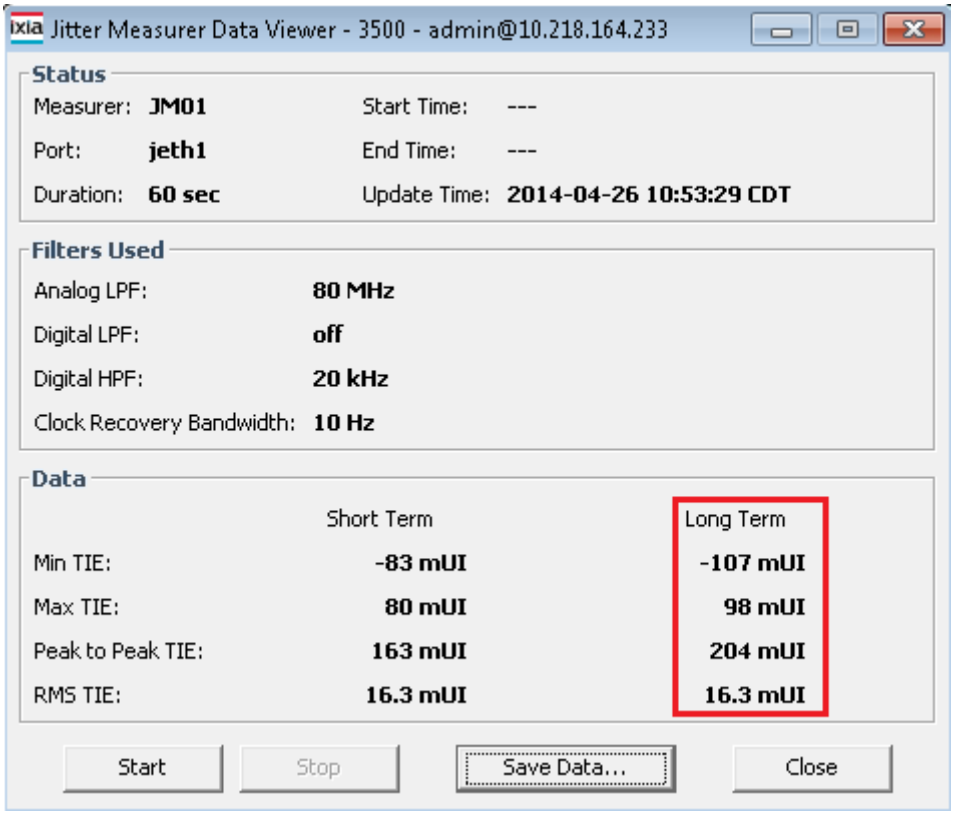
Test Variables

Repeat the test with the following variations:

- Test multiple Ethernet speeds (1G, 10G) and on all supported optical interfaces (SX, LX, KX, EX etc.)

Results Analysis

After 60 seconds the test completes. Verify that Long Term Peak to Peak TIE is <0.5 UI after 60 seconds. This corresponds to 400ps for 1G and 48.485ps for 10G.



Conclusions

ITU-T G.8262 section 8.3 provides requirements for testing jitter compliance for Synchronous Ethernet clocks. These tests must be completed for Synchronous Ethernet equipment and Ixia 3500 has the accuracy and precision to accomplish this task.

Test Case: Jitter Tolerance

Overview

The EEC is required to tolerate certain input jitter conditions without causing a failure of operation of the device. ITU-T G.8262 section 9.2 provides test parameters to evaluate the tolerance of an EEC to input jitter. Jitter Tolerance verifies that a device can tolerate sufficient levels of jitter without failure.

Objective

This test verifies that the DUT can tolerate the levels of jitter that may be present in the network without causing failure of the synchronization system.

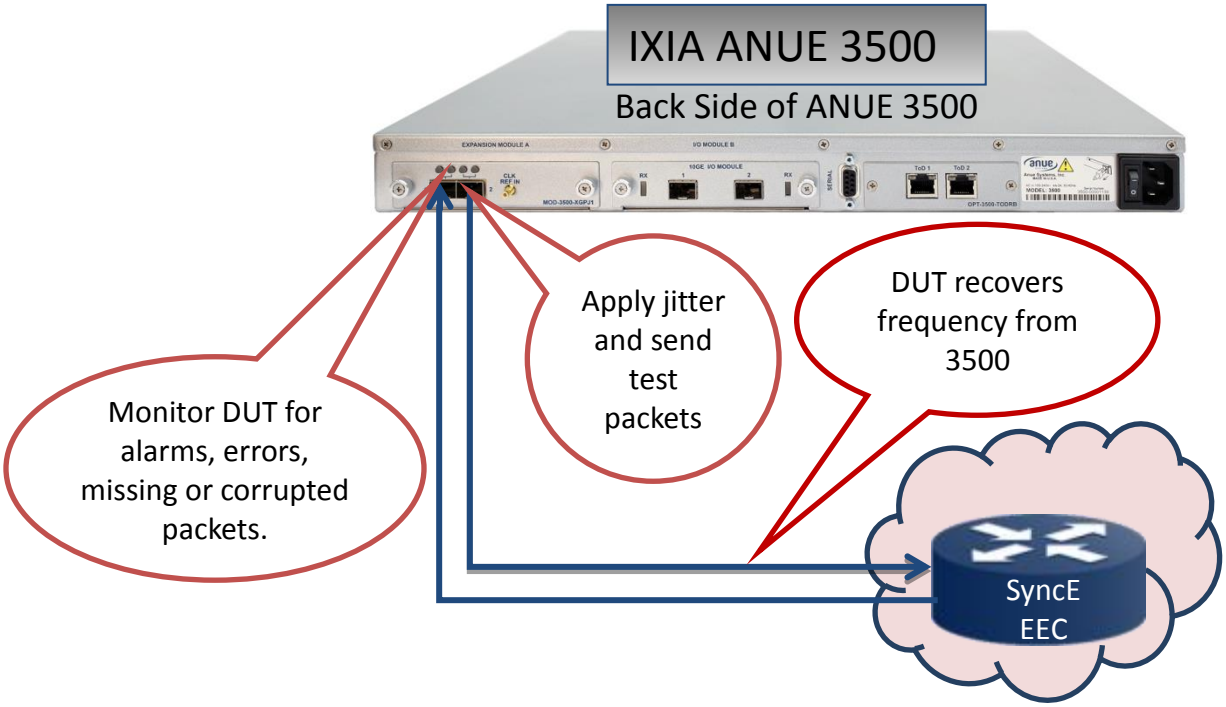
The jitter introduced to the DUT (input jitter) must not cause any of the following:

- Any lost or corrupted packets at the 3500
- Any clock switch event or alarms/errors detected by the DUT such as CRC errors or LOF

For the jitter tolerance test, jitter is generated by the Anue 3500. Evaluation of passing and failing is accomplished by observing the DUT alarms, clock status, and corruption of the packets being looped back.

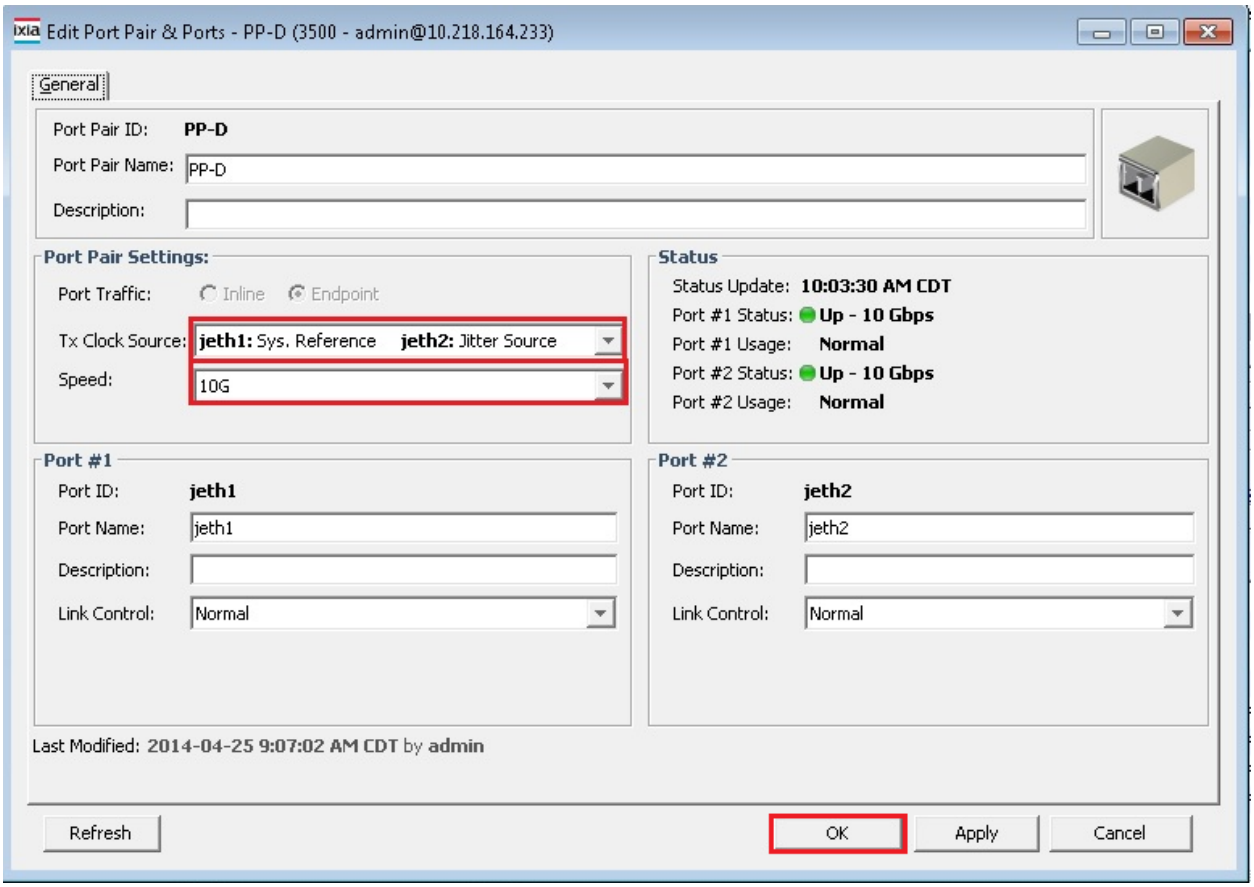
For additional details, see ITU-T G.8262, section 9.2 jitter tolerance.

Setup

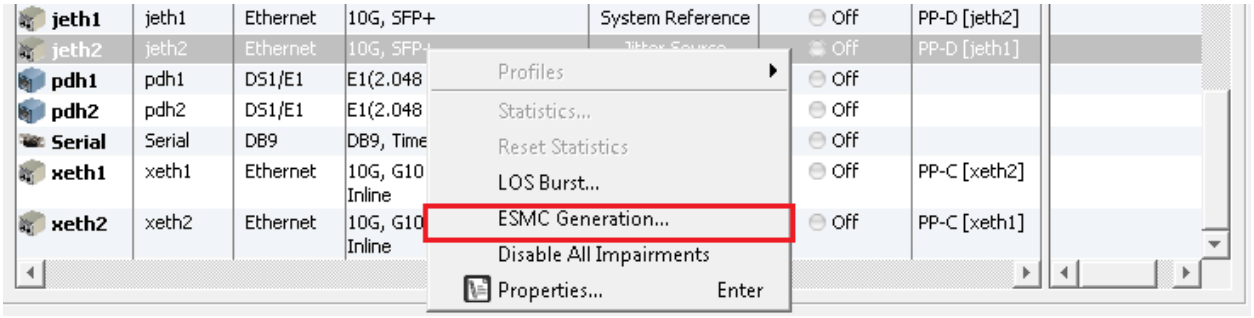

IXIA ANUE 3500
Back Side of ANUE 3500
Monitor DUT for alarms, errors, missing or corrupted packets.
Apply jitter and send test packets
DUT recovers frequency from 3500
SyncE EEC

Step-by-Step Instructions

1. Click on ports and select jeth1. Double click to launch ‘Port Properties’ dialog. In the ‘Port Pair Settings’:
    - Set ‘Tx Clock Source’ to “jeth1: Sys Reference jeth2: Jitter Source”
    - Set ‘Speed’ to “10G”
    - Click OK.

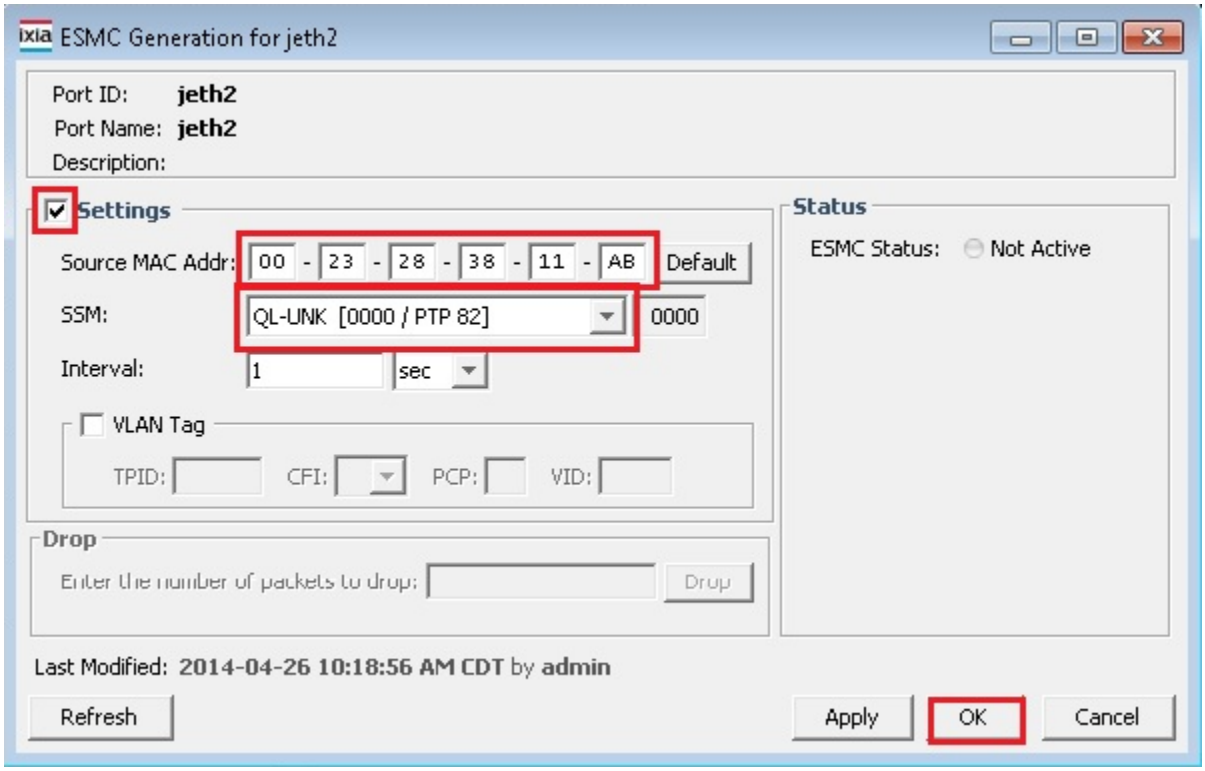


2. Select jeth2 in the ports view and right click.
    - Select ‘ESMC Generation’ from the menu.

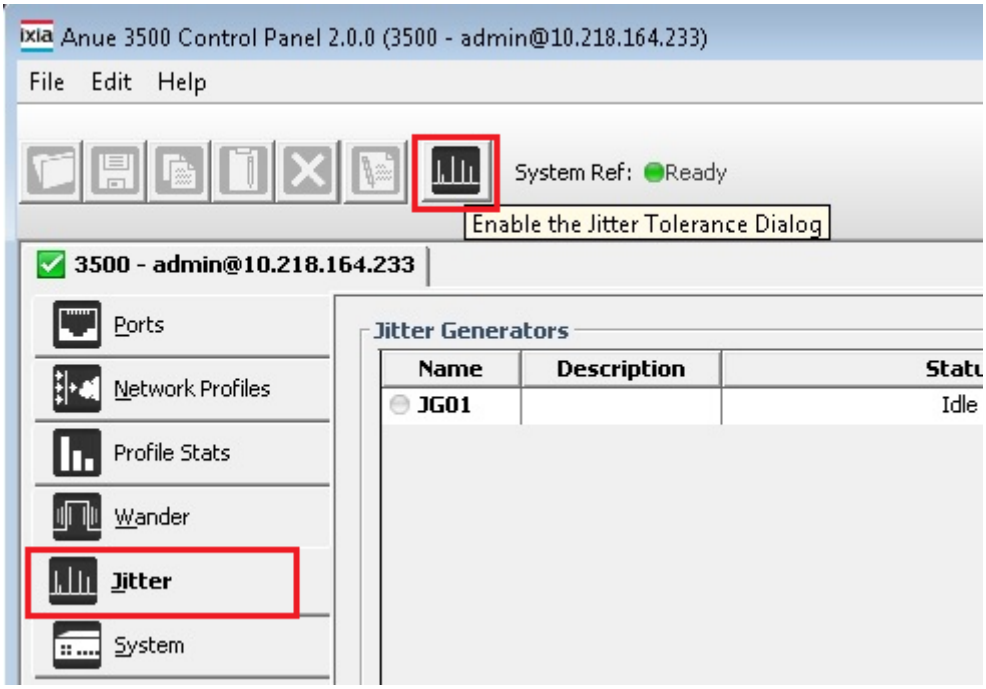


    - In the ‘ESMC Generation’ dialog, select the checkbox next to ‘Settings’. Optionally, configure the ‘Source MAC Addr’and ‘SSM’.

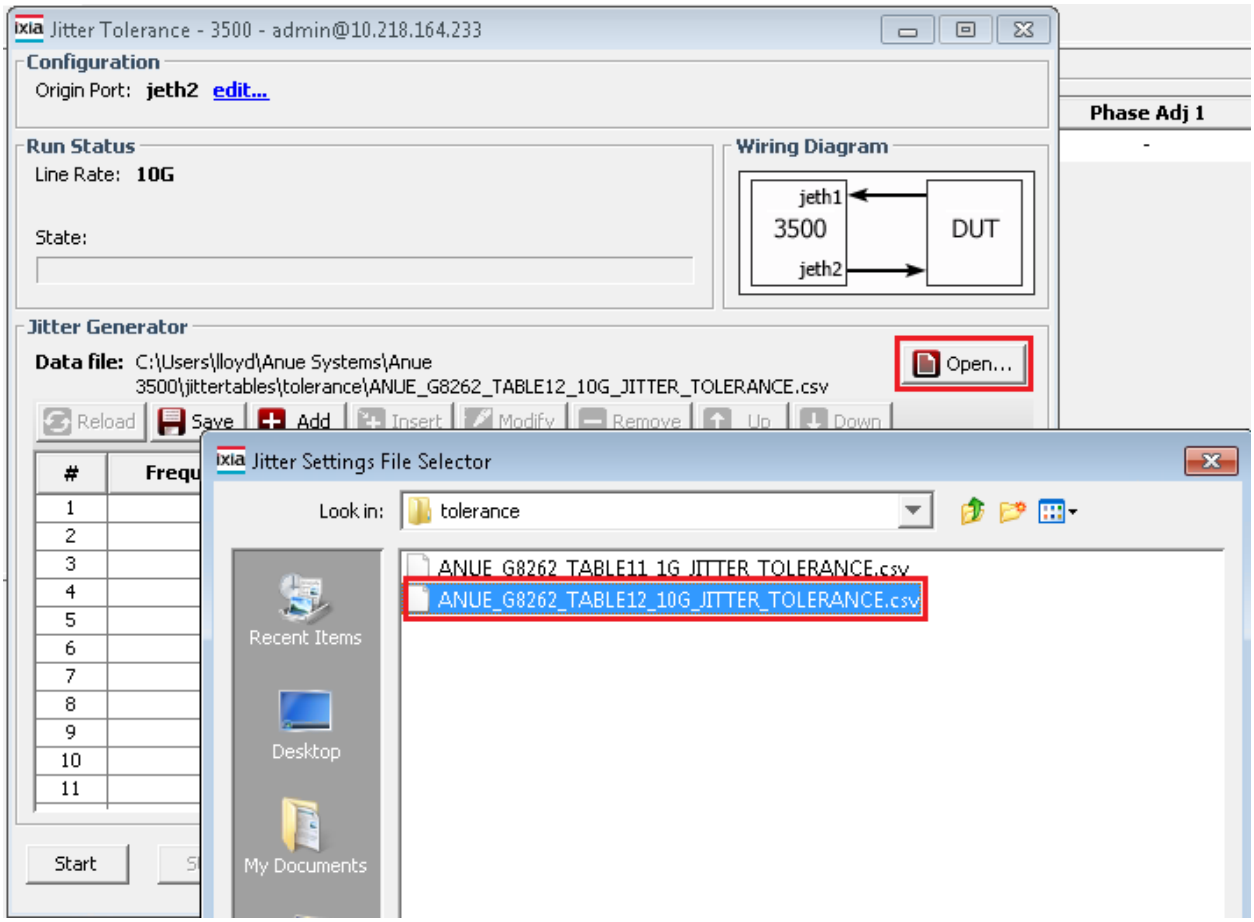
- Click OK.



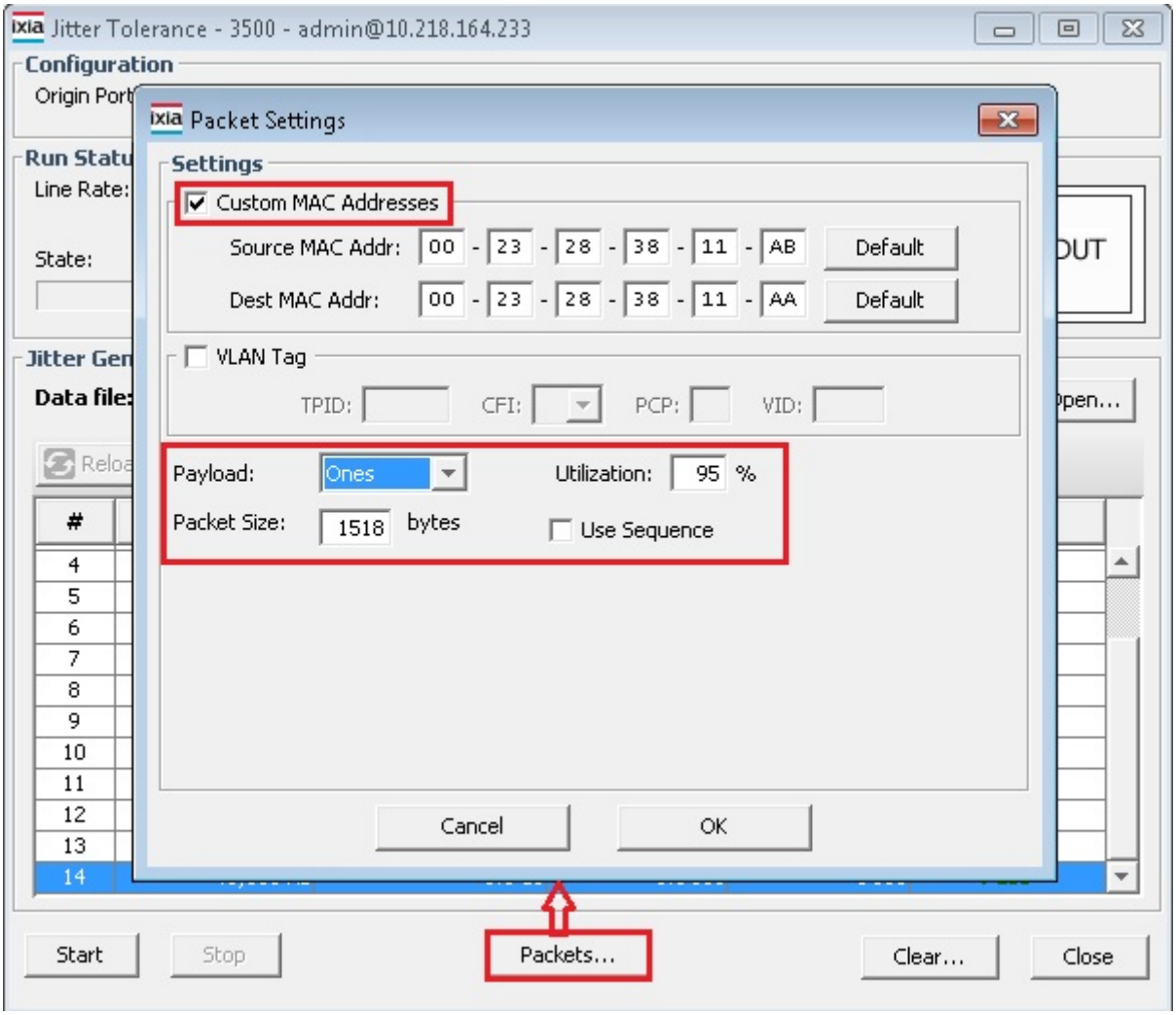
3. Click on jitter in the left side menu.
   - Click on 'Jitter Tolerance' icon at top.



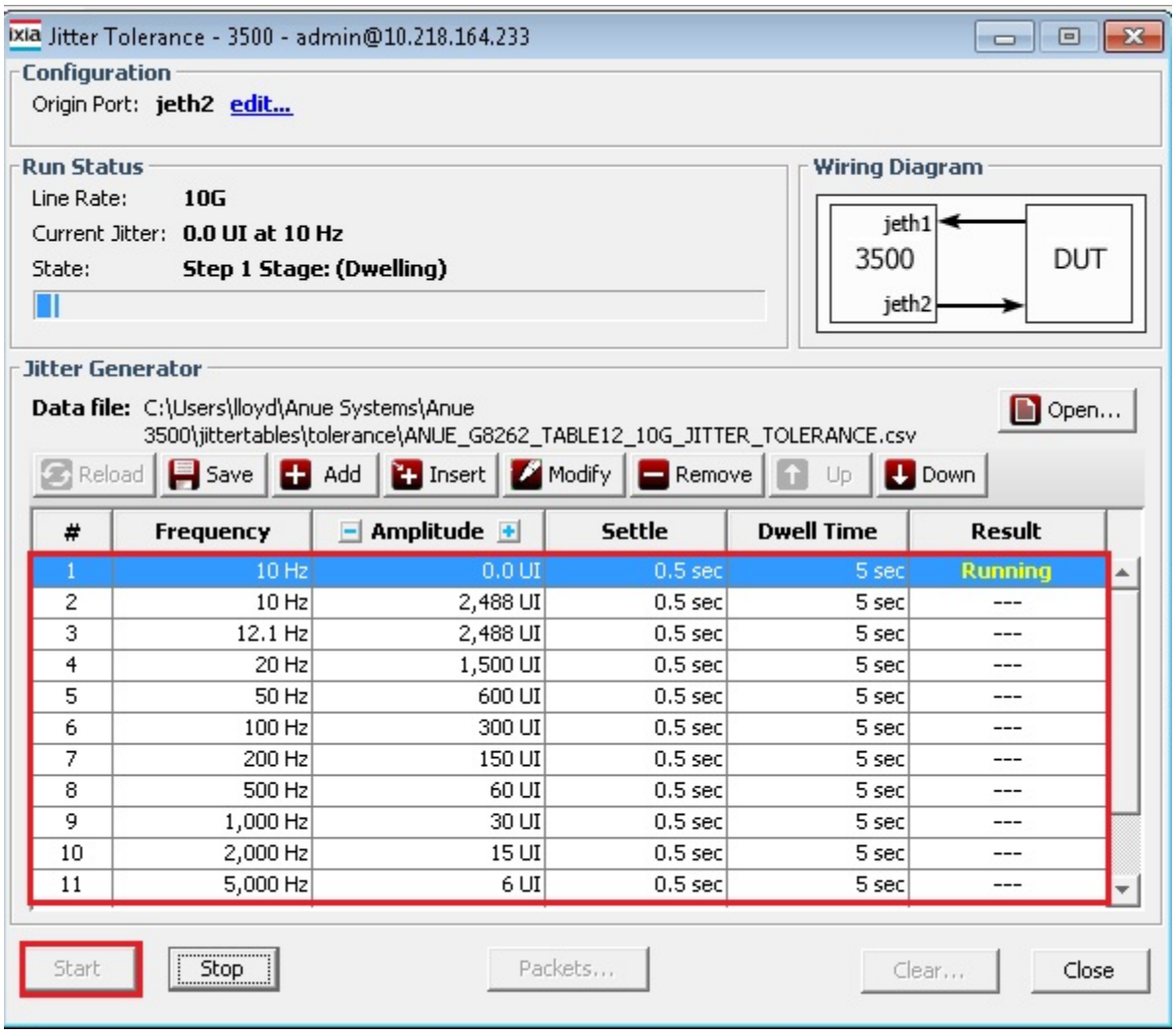
- ‘Open’ the appropriate 1G or 10G jitter input table file in the ‘Jitter Tolerance’ dialog.



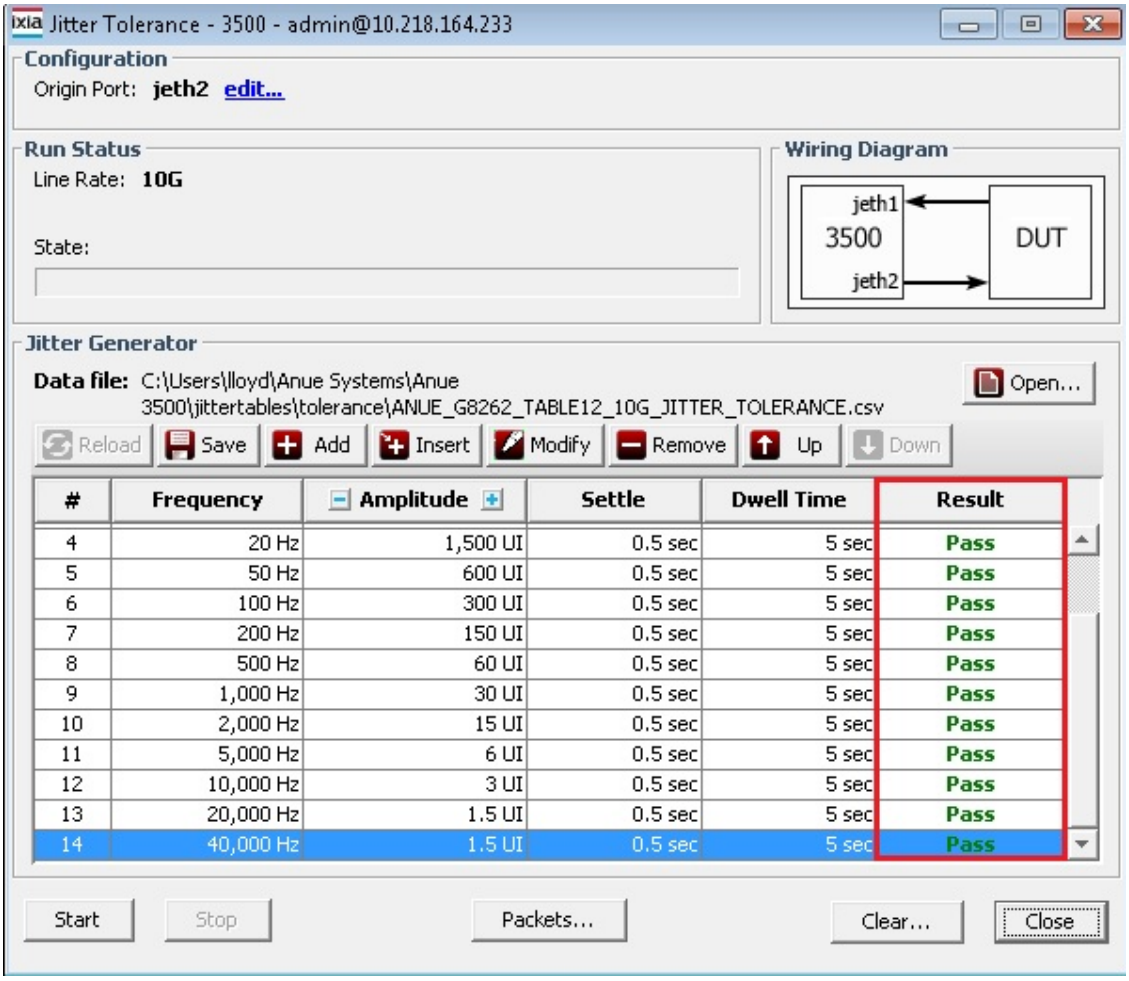
4. After the file is opened successfully i.e. the values are displayed in the columns ‘Frequency’, ‘Amplitude’, ‘Settle’, ‘Dwell’ etc., then click on ‘Packets...’.
   - In the dialog, configure the MAC addresses and payload properties.
   - Click ‘OK’ to apply the settings.



5. Click on ‘Start’ to start the tolerance test.
    - Configure DUT to switch/route test stream back to jeth1



6. Observe that:
   - Verify all frequency test points pass (Ixia 3500)
   - Verify errors/alarms at DUT



#	Frequency	Amplitude	Settle	Dwell Time	Result
4	20 Hz	1,500 UI	0.5 sec	5 sec	Pass
5	50 Hz	600 UI	0.5 sec	5 sec	Pass
6	100 Hz	300 UI	0.5 sec	5 sec	Pass
7	200 Hz	150 UI	0.5 sec	5 sec	Pass
8	500 Hz	60 UI	0.5 sec	5 sec	Pass
9	1,000 Hz	30 UI	0.5 sec	5 sec	Pass
10	2,000 Hz	15 UI	0.5 sec	5 sec	Pass
11	5,000 Hz	6 UI	0.5 sec	5 sec	Pass
12	10,000 Hz	3 UI	0.5 sec	5 sec	Pass
13	20,000 Hz	1.5 UI	0.5 sec	5 sec	Pass
14	40,000 Hz	1.5 UI	0.5 sec	5 sec	Pass

Test Variables

Repeat the test with the following variations:

- Test multiple Ethernet speeds (1G, 10G) and on all supported optical interfaces (SX, LX, KX, EX etc.)
- Optional VLAN for test packets
- Test packet payload size: random, zeroes, ones, increment, decrement, custom
- Bandwidth utilization: 1-100% in 1% increments
- Frequency Test Points using different CSV input files

Results Analysis

The test fails if there is any occurrence of the following while monitoring the DUT:

- Alarms (to be observed at DUT)
- Clock switch events (to be observed at DUT)
- Missed or corrupted packets are received on jeth1 (to be observed on ANUE 3500)

Conclusions

ITU-T G.8262 section 9.2 provides requirements for testing jitter tolerance for Synchronous Ethernet clocks. These tests must be completed for Synchronous Ethernet equipment and Ixia 3500 has the accuracy and precision to accomplish this task.

Devices and Topologies

Test Case: Boundary Clocks - PTP Timestamp Accuracy (Time Error)

Overview

Boundary Clocks are PTP devices that have a slave port from which they recover a clock, and one or more master ports that provide PTP timestamps for downstream devices by using the clock recovered from the slave port. These devices may introduce non-linear timing impairments that resemble PDV when introduced into a network. It is important to measure this PDV-like effect to characterize a boundary clock and consider its impact on a timing network.

Boundary Clocks may also have recovered clock interfaces such as T1/E1 or 2.048MHz that provide the recovered clock. In that case, these interfaces may be measured and the boundary clock is treated as an ordinary clock or slave clock for the purpose of evaluating recovered clock accuracy. However, the impairment created on the master ports should still also be evaluated independently from the frequency accuracy.

Objective

This test evaluates the Time Error of a PTP Boundary Clock by analyzing the accuracy of the time stamps in sync and follow-up packets produced on the DUT's master ports.

***Note**: This testing requires that the Anue 3500 have two Ethernet port pairs for a total of four Ethernet ports.*

Setup

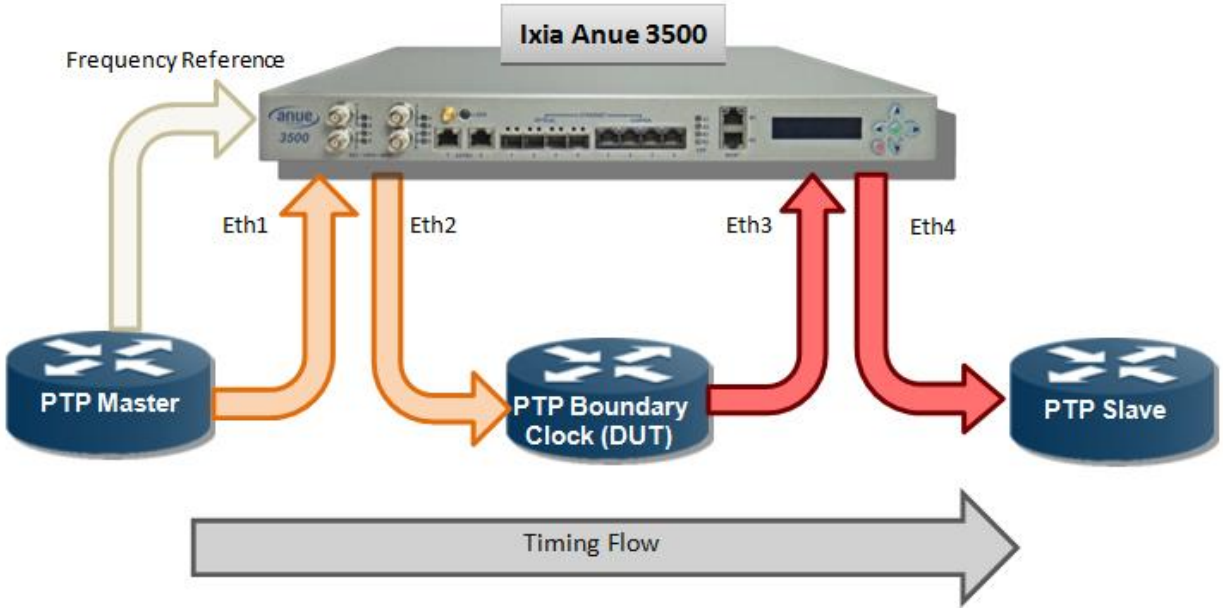
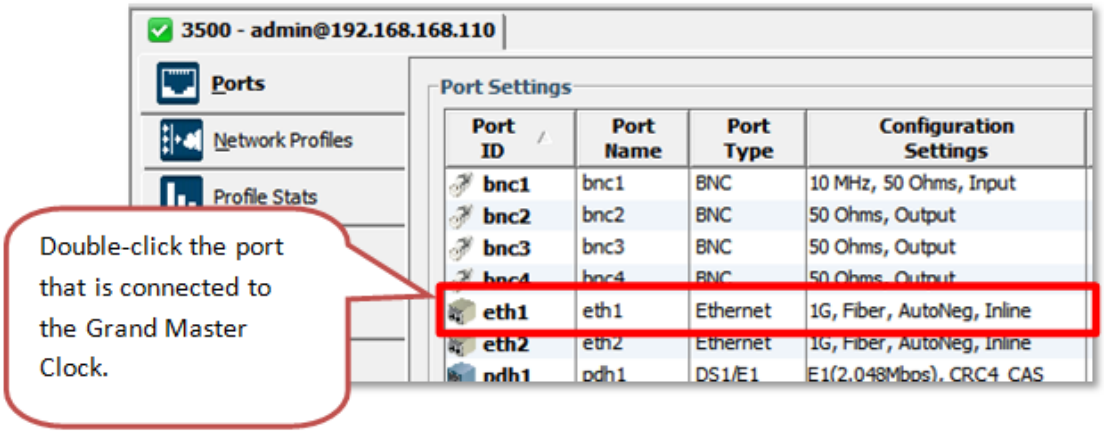
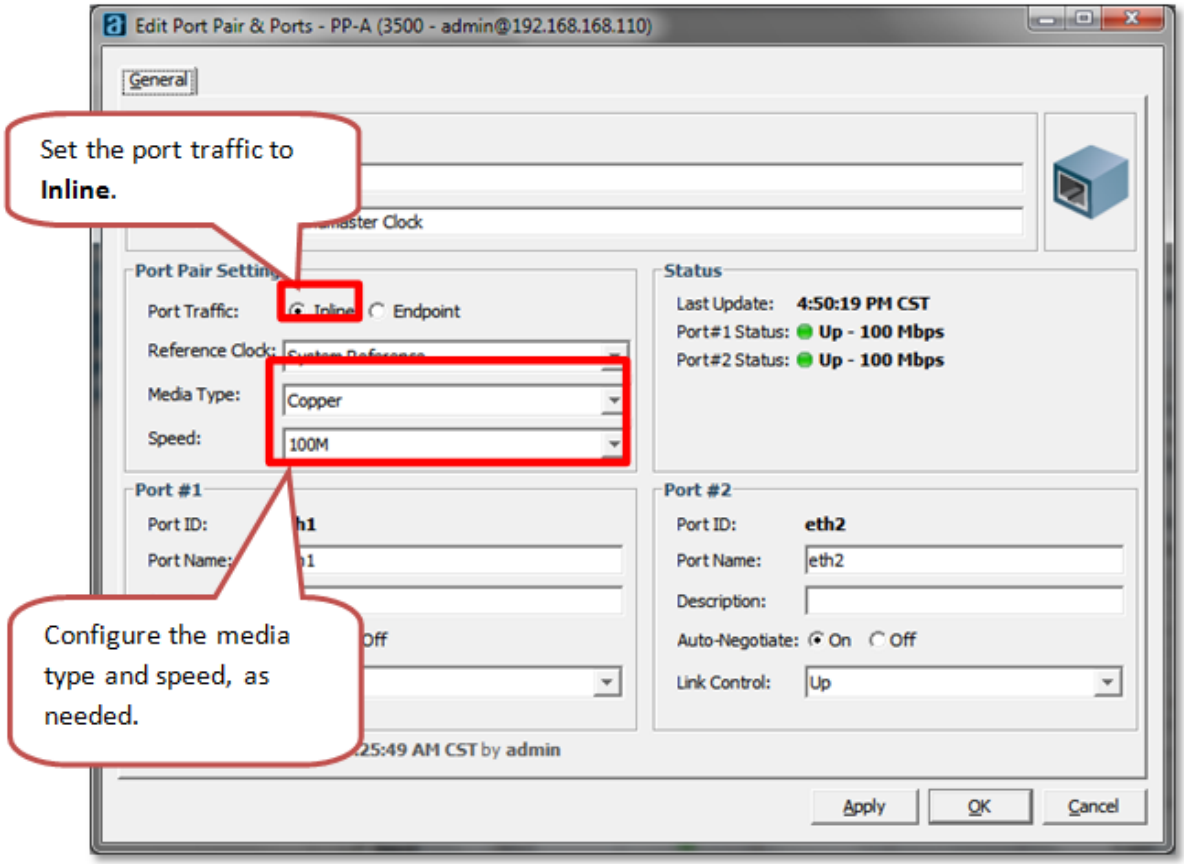


Figure 65. Boundary Clock Test Setup

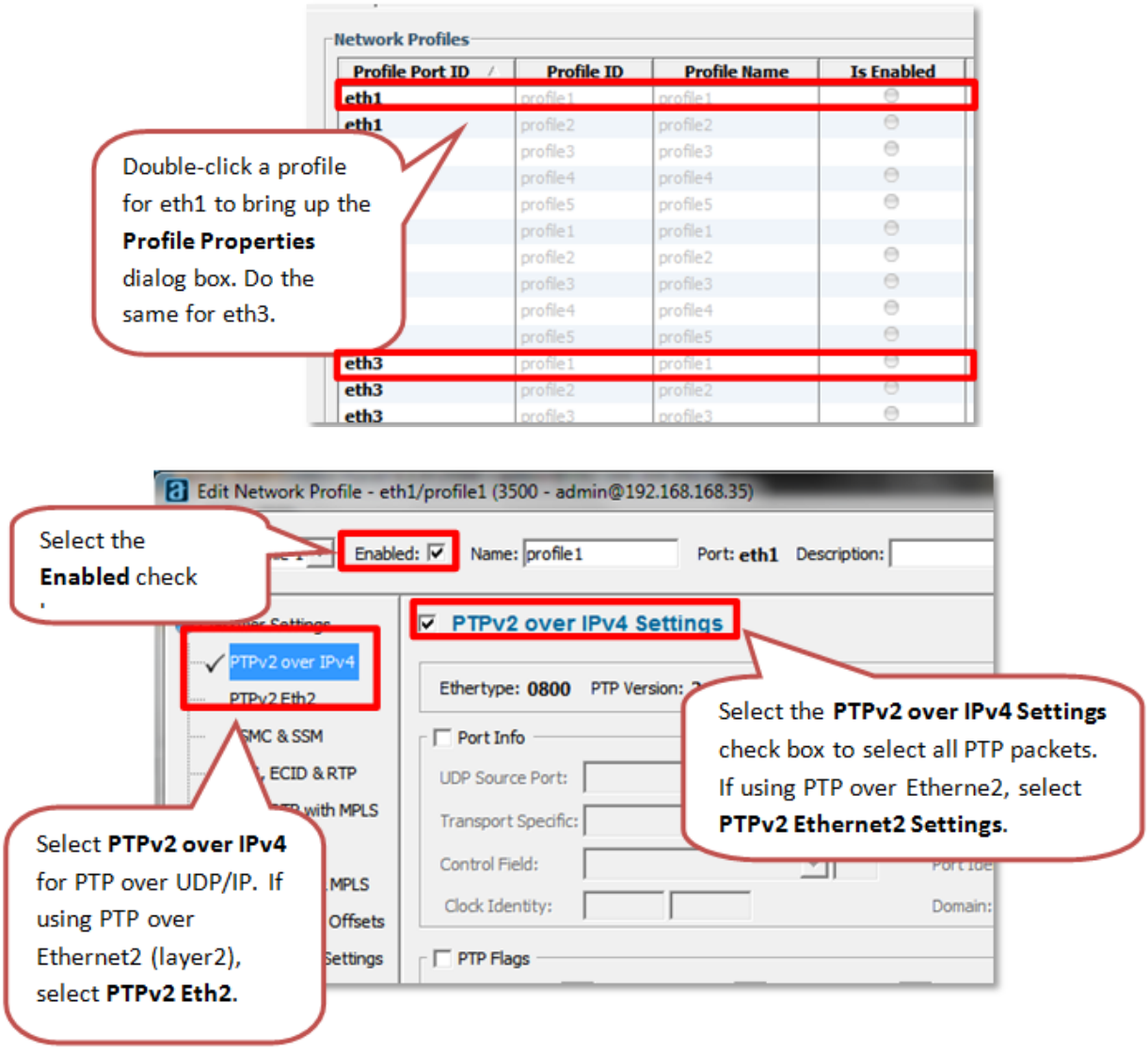
1. Connect the DUT Boundary Clock, Grand Master clock, and PTP Slave Clock to the Anue 3500 as shown in the test setup drawing:
    a. Connect the Anue 3500 Eth1 interface to the Grand Master Clock or PTP Master Ethernet interface.
    b. Connect the Anue 3500 Eth2 interface to the DUT Boundary Clock's slave interface.
    c. Connect the Anue 3500 Eth3 interface to the DUT Boundary Clock's master interface.
    d. Connect the Anue 3500 Eth4 interface to the PTP Slave interface.
    Note: Any mixture of 1GB optical or copper, or 1G and 10G interfaces is supported. For example. the Grand Master to DUT can be connected on 10G, and the DUT to slave can be 1G.
2. Configure two port-pairs on the Anue 3500 for 'Inline' mode, and if using 1G dual-media ports, configure for the correct media type and speed (copper or fiber, 100M or 1G) by using the Anue 3500 Control Panel Ports tab. Double-click one of the ports in the port pair that is connected between the Grand Master Clock and the DUT Boundary Clock. This brings up the **Ethernet Port Property** dialog box.





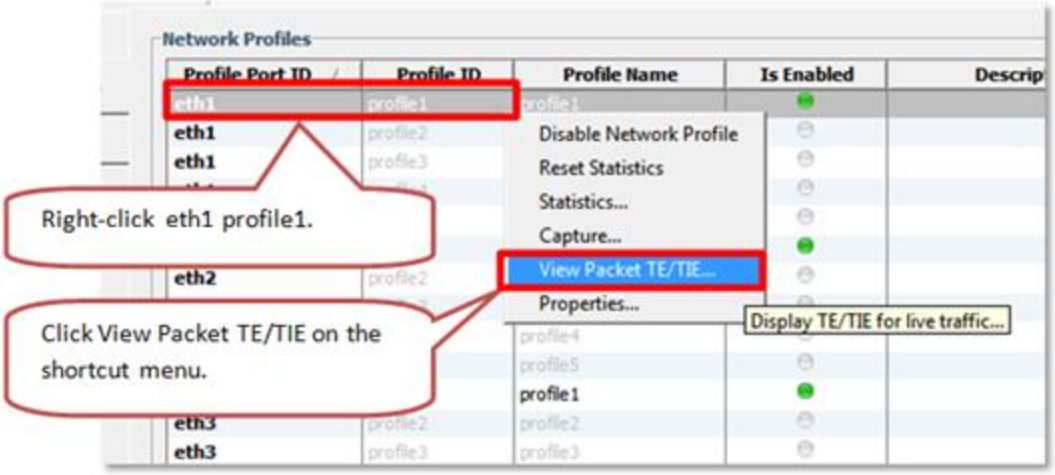
Repeat this process for the port pair that is connected between the DUT Boundary Clock and the Slave Clock.

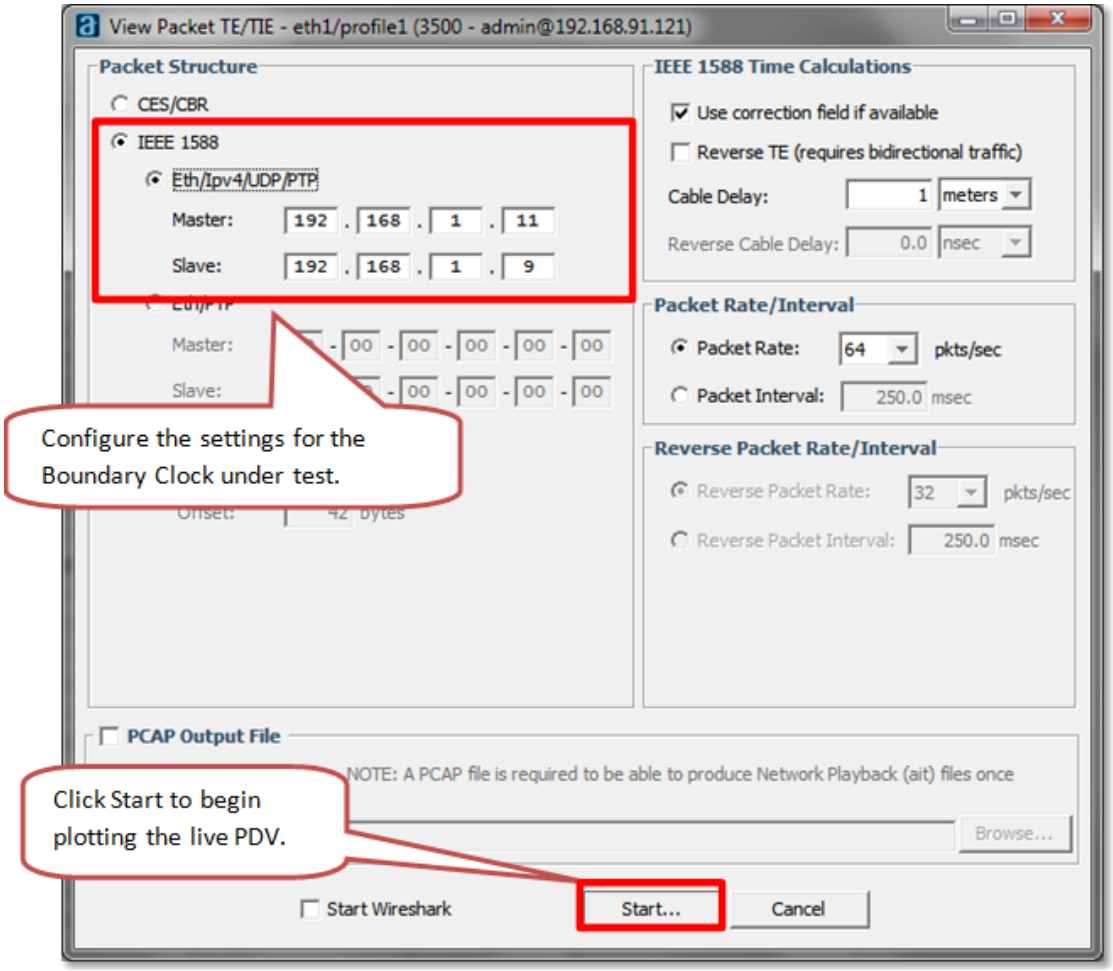
3. Configure Network Profiles for each port used in the test to match the PTP packets. Configure the classifier for PTP for the port connected to the Grand Master Clock (for example, eth1) and also for the port connected to the master port side of the Boundary Clock DUT (for example, eth3). *Note: You must do this procedure for both the port connected to the DUT as well as the port connected to the Grand Master Clock.*


Network Profiles
Profile Port ID
Profile ID
Profile Name
Is Enabled
eth1
eth3
Double-click a profile for eth1 to bring up the **Profile Properties** dialog box. Do the same for eth3.
Edit Network Profile - eth1/profile1 (3500 - admin@192.168.168.35)
Enabled:
Name: profile1
Port: eth1
Description:
PTPv2 over IPv4 Settings
PTPv2 over IPv4
PTPv2 Eth2
Ethertype: 0800
PTP Version:
Port Info
UDP Source Port:
Transport Specific:
Control Field:
Clock Identity:
Domain:
PTP Flags
Select the **Enabled** check
Select **PTPv2 over IPv4** for PTP over UDP/IP. If using PTP over Ethernet2 (layer2), select **PTPv2 Eth2**.
Select the **PTPv2 over IPv4 Settings** check box to select all PTP packets. If using PTP over Etherne2, select **PTPv2 Ethernet2 Settings**.

Step-by-Step Instructions

1. Begin live PDV on both eth1 and eth3 profiles in the **Network Profile** window.





Repeat the same process for eth3 profile1.

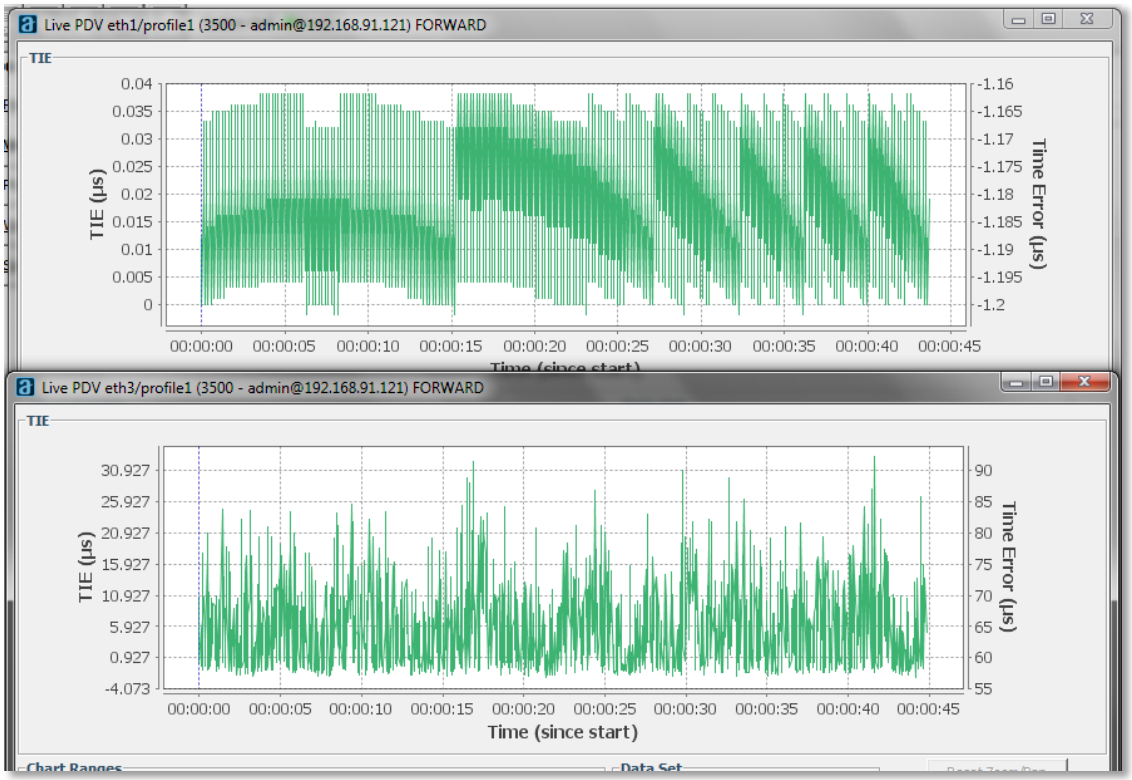
Test Variables

Repeat the test with the following variations:

- Test with the system in both PTP **multicast** mode and in PTP **unicast** mode.
- Test with the system in both **one-step mode** (which reduces the number of messages) and in **two-step mode**.
- Test using varying sync and follow-up packet rates on both sides of the boundary clock, for example:
    - 1 packet/sec from master to BC, 64 packets/sec from BC to slaves
    - 4 packets/sec from master to BC, 1 packet/sec from BC to slave
- Test multiple Ethernet speeds and on all supported interfaces (10G, 1G, and copper/optical); especially, testing dissimilar speeds or interfaces on each side of the BC, such as 10G from master to BC and 1G from BC to slaves.

Results Analysis

1. Review the PDV on eth3 compared to eth1's PDV. This indicates the insertion properties of the Boundary Clock.



Conclusions

Because the goal of boundary clocks in the network is to improve time synchronization across a packet network, it is critical to evaluate the time error or time accuracy of the boundary clock before deployment.

Test Case: Transparent Clocks – Correction Field Accuracy

Overview

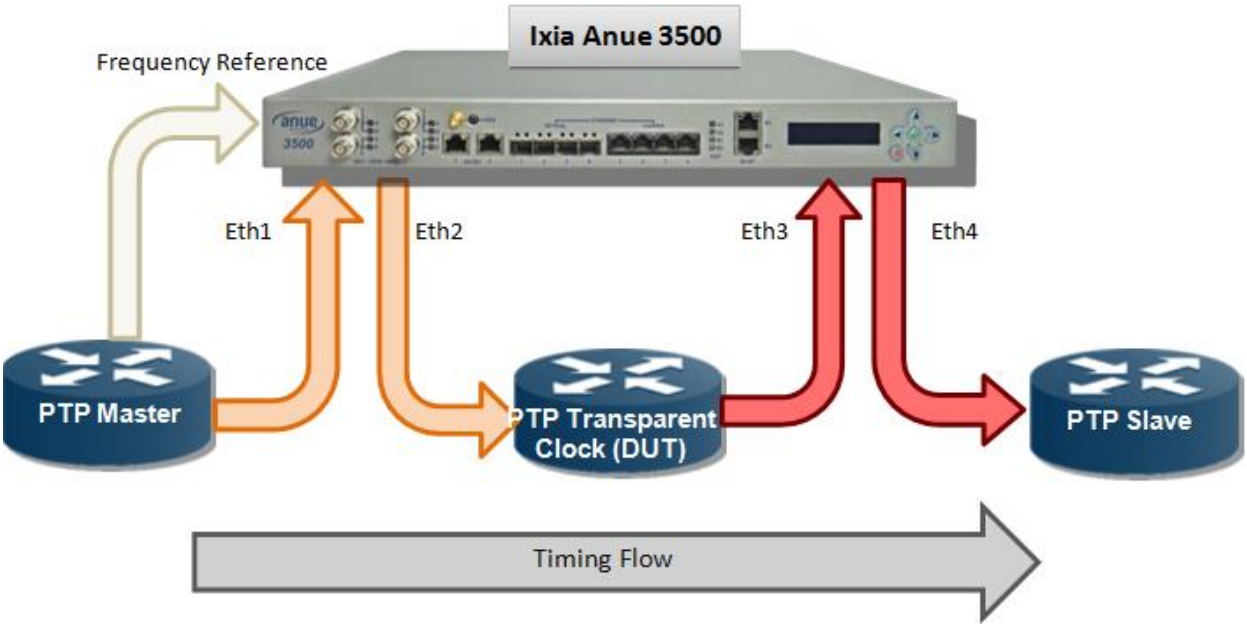
Transparent Clocks are PTP devices that pass forward PTP packets from one port to another, while updating the PTP packet's *correction field* by adding the residence time (time the packet spends in the Transparent Clock) to the value in the correction field. The PTP correction field contains the amount of time a PTP packet spent within the transparent clock switch. This allows the slave clock to compensate for the PDV caused by all the transparent clocks in the PTP network path. It is important to measure the accuracy of the correction field as updated by the transparent clock.

Objective

This test measures the accuracy of the correction field updates in sync and follow-up packets provided by a PTP Transparent Clock.

Note: This testing requires that the Anue 3500 have two Ethernet port pairs for a total of four Ethernet ports.

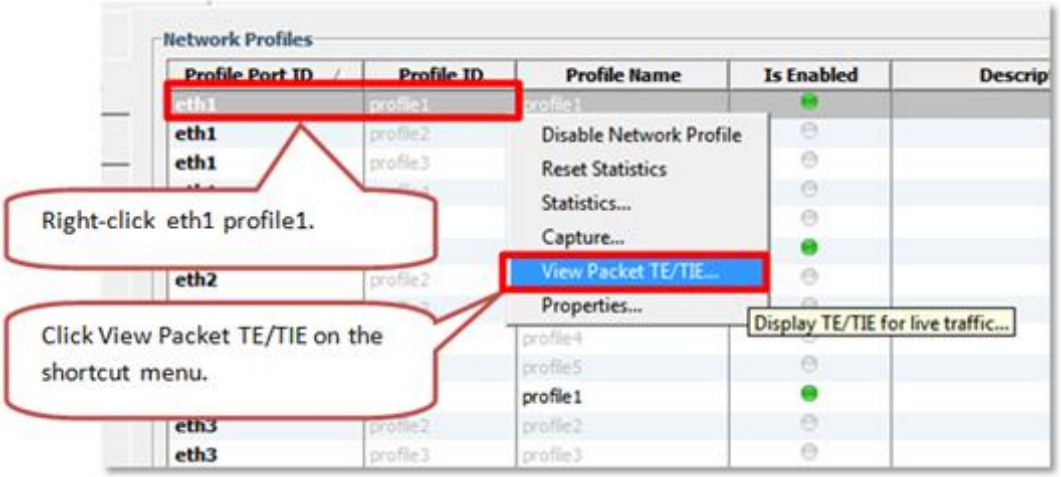
Setup

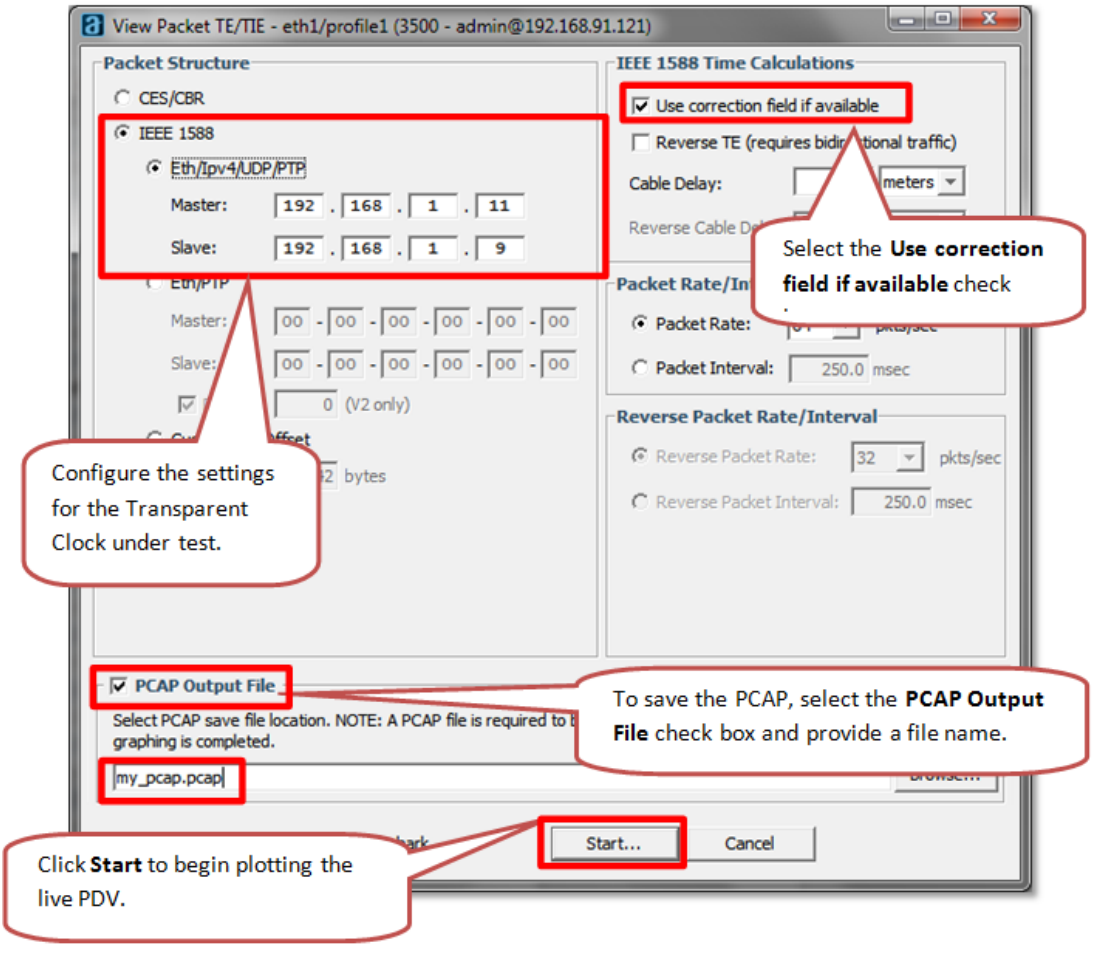


Test setup for the Transparent Clock test is identical to the Boundary Clock Test Setup. Complete the steps in *Boundary Clock Test Setup*.

Step-by-Step Instructions

1. Begin live PDV on both eth1 and eth3 profiles in the **Network Profile** window.





Repeat the same process for eth3 profile1.

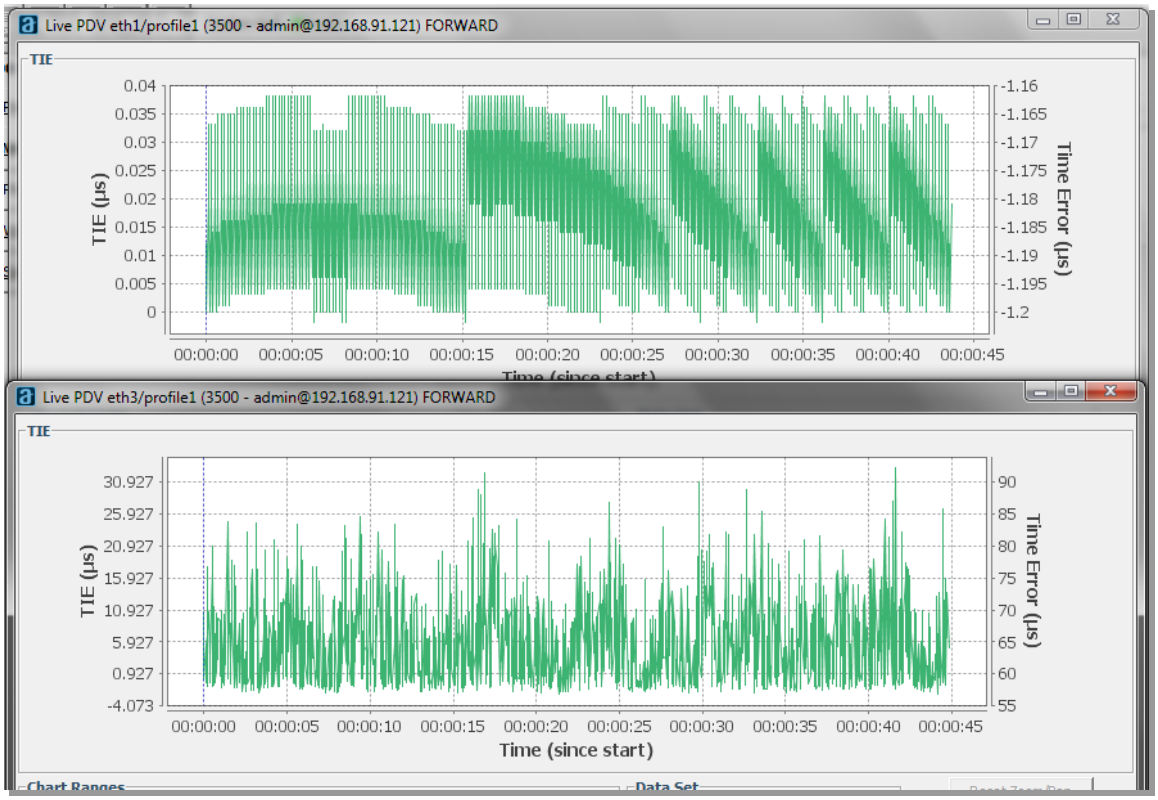
Test Variables

Repeat the test with the following variations:

- Test with the system in both PTP **multicast** mode and in PTP **unicast** mode.
- Test with the system in both **one-step mode** (which reduces the number of messages) and in **two-step mode**.
- Test using varying sync and follow-up packet rates or different PTP profiles as supported by the grand master and slave clocks.
- Test multiple Ethernet speeds and on all supported interfaces (10G, 1G, and copper/optical); especially, testing dissimilar speeds or interfaces on each side of the TC, such as 10G from master to TC and 1G from TC to slaves; note that this rate adaptation in the TC may cause a time error offset that may manifest as an inaccuracy in the 1PPS recovered on the slave clock.

Results Analysis

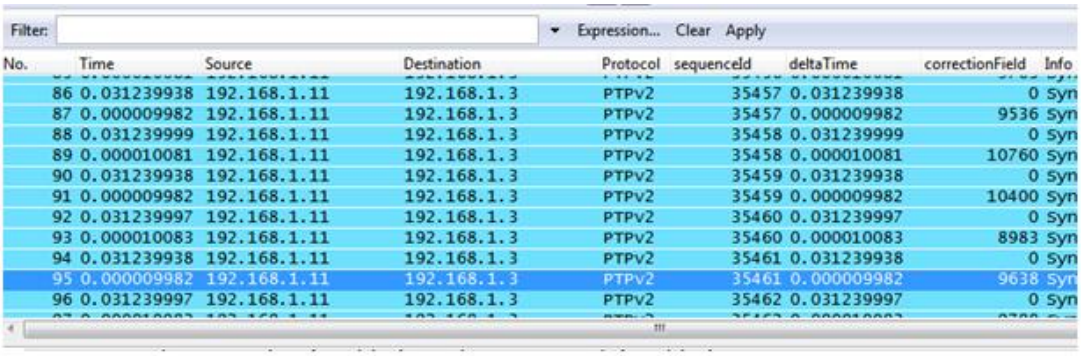
1. Review the PDV on eth3 compared to eth1's PDV, with the PDV of eth3 by using the correction field to compensate for the residence time. This indicates the error or inaccuracy in the Transparent Clock's correction field updates.



2. For a precise numerical evaluation, use Anue Wireshark to compare the actual delay of each packet with the correction field value.

a. Using Anue Wireshark, open the Master-side PCAP file specified when the Live PDV view was opened on eth1/profile1.
b. In Anue Wireshark, click **File** > **Merge**, and then select the Slave-side PCAP file specified when the Live PDV view was opened on eth3/profile1. Be sure and click **Merge Packets Chronologically**.

c. On the **Edit** menu, click **Preferences**. When the **Preferences** window opens, under **User Interface**, click **Columns**. Add three new columns:
    i. Title: suquenceId, Field type: Custom, Field name: ptp.v2.sequenceid
    ii. Title: deltaTime, Field type: Delta Time
    iii. Title: correctionField, Field type: Custom, Field name: ptp.v2.correction.ns
    iv. Click **OK**.
d. Click the **Time** column header to sort the packets in order of time.
e. Locate the packets with duplicate sequenceId fields; these indicate the packets that were processed through the boundary clock. Find the packet with the correctionField and compare the correctionField vaue with the deltaTime value. Note the deltaTime is in seconds, while the correctionField is in nanoseconds.



Conclusions

Because the goal of transparent clocks in the network is to mitigate PDV introduced by switches by adding an accurate correction field value, the accuracy of the correction field must be evaluated

Test Case: Hybrid SyncE and PTP - SyncE Islands with PTP Connection

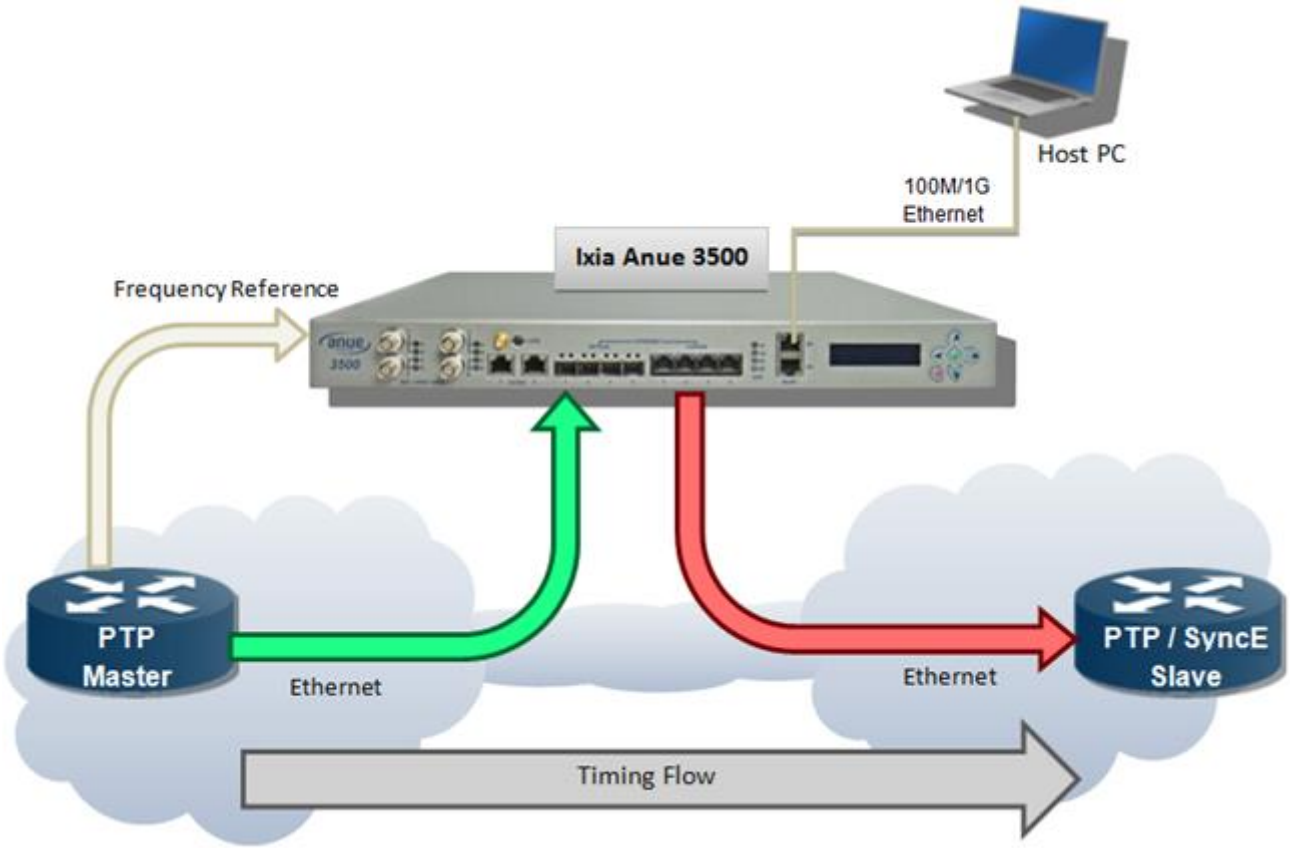
Overview

Timing over Packet networks may use a combination of PTP and Synchronous Ethernet (SyncE), where frequency and phase synchronization are delivered across a packet network by using PTP, and the frequency recovered at the slave (or boundary clock) is delivered on SyncE interfaces. Testing these hybrid networks is accomplished by measuring the recovered clock on the slave DUT on the SyncE interface while the specified packet impairment is being introduced between the Grand Master and the DUT.

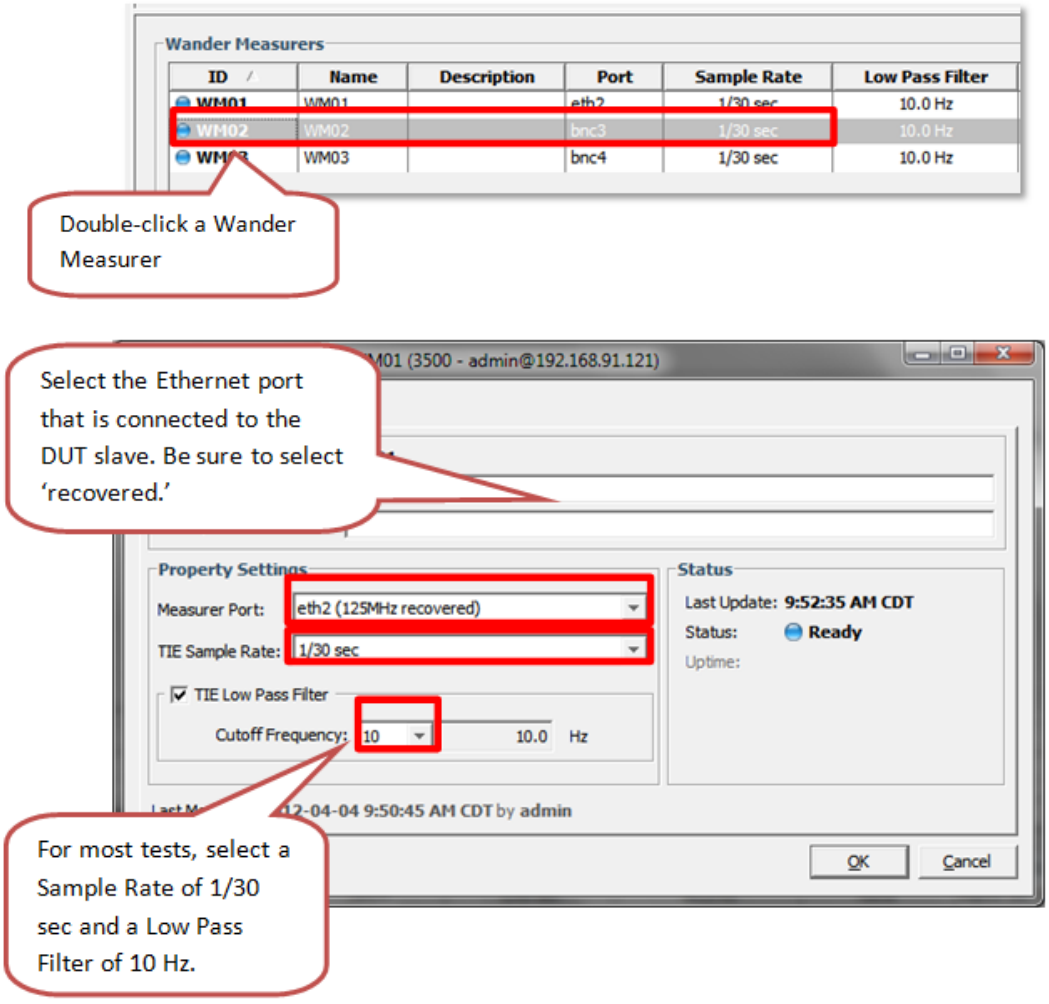
Objective

This test evaluates the performance of SyncE frequency recovered from a PTP network in the presence of packet-layer impairment.

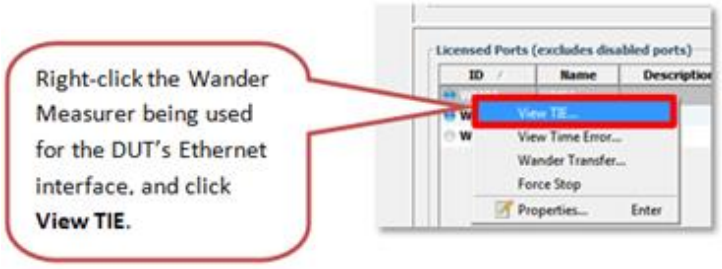
Setup

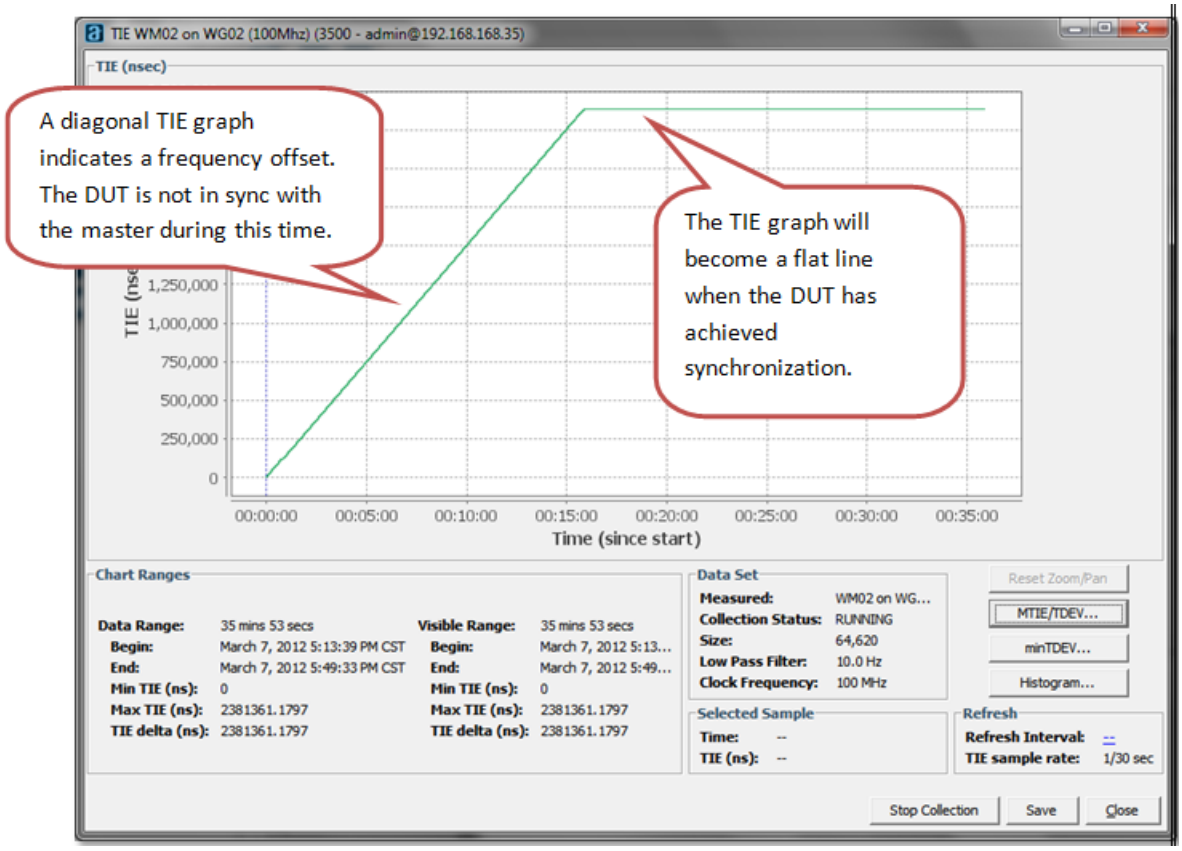


1. Testing and setup is identical to previous section *G.8261 Testing Timing Over Packet,* with the exception of the choice of recovered clock interface, and the selection of masks for measurement of this clock. Complete the setup steps from section *G.8261 Testing Timing Over Packet* with the following variations.
2. The Slave's recovered clock is measured on the Ethernet interface that is connected between the 3500 and the DUT. Select a Wander Measurer from the Anue 3500 Control Panel's Wander tab to measure the DUT's Ethernet interface. Configure the Wander Measurer for the correct interface.



3. The PTP Slave DUT may take up to an hour or longer to synchronize with the Grand Master Clock. You can identify synchronization by monitoring the DUT's Ethernet clock TIE graph, and also by monitoring the user interface for indication of synchronization.





4. After the DUT is in sync with the Grand Master, close the TIE window and restart the TIE measurement.

Step-by-Step Instructions

1. Test steps are the same as in the previous section *G.8261 Testing Timing Over Packet*

Test Variables

None

Results Analysis

1. Results are the same as in the previous section *G.8261 Testing Timing Over Packet,* only differing in the masks chosen for SyncE measurements in the MTIE/TDEV window.

Conclusions

As synchronization quality requirements are becoming more strict in next-generation networks, hybrid networks using SyncE and PTP are becoming more common. It is important to measure the quality of synchronization in equipment used in these next-generation networks.

Test Case: Hybrid SyncE and PTP - SyncE Frequency and PTP Time

Overview

Synchronous Ethernet (SyncE) may be used to deliver frequency synchronization on networks in conjunction with PTP used for Phase or Time of Day delivery. In this type of network, only Ethernet interfaces are used. The Anue 3500 supports a variety of testing these combination networks with physical layer (SyncE) and packet layer (PDV) measurement and impairment conducted simultaneously.

Objective

This test evaluates the ability of hybrid SyncE/PTP equipment to provide frequency synchronization over SyncE and Time synchronization over PTP.

Setup

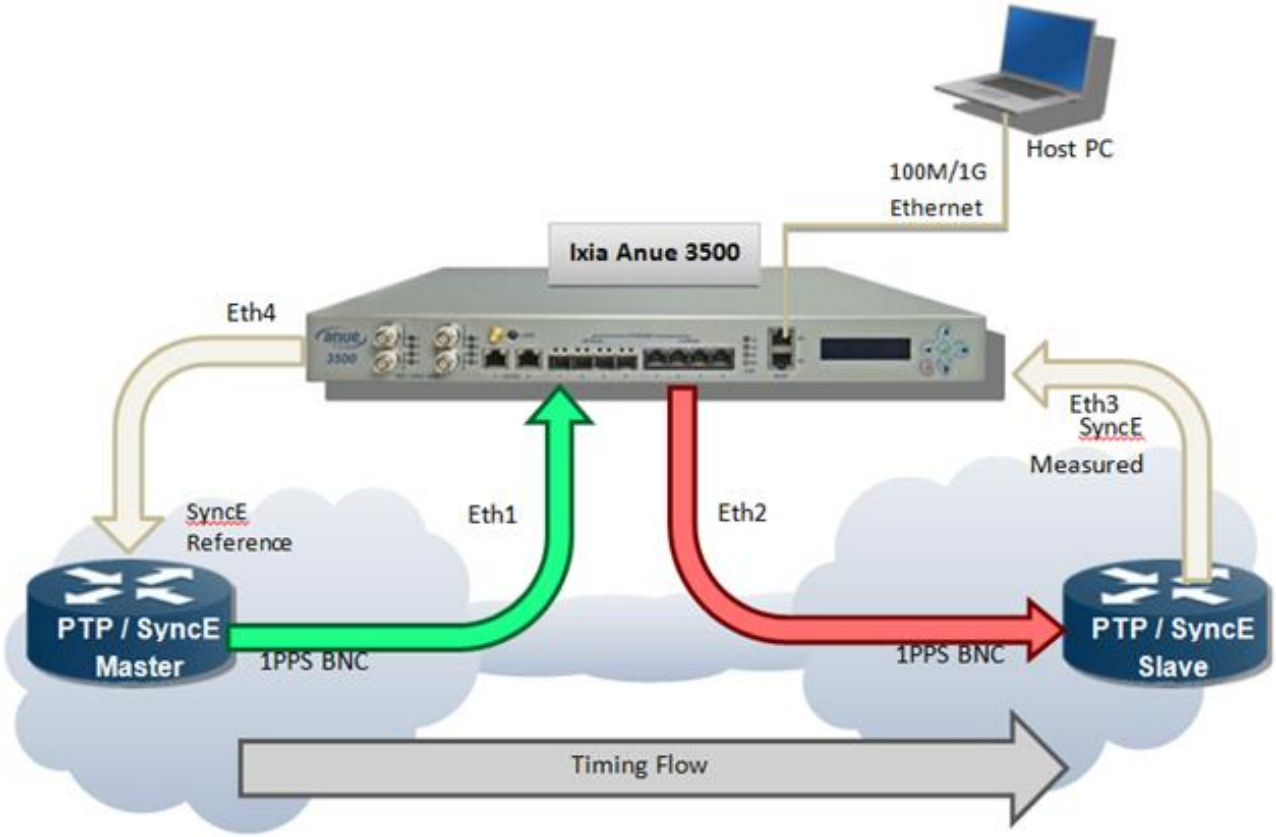
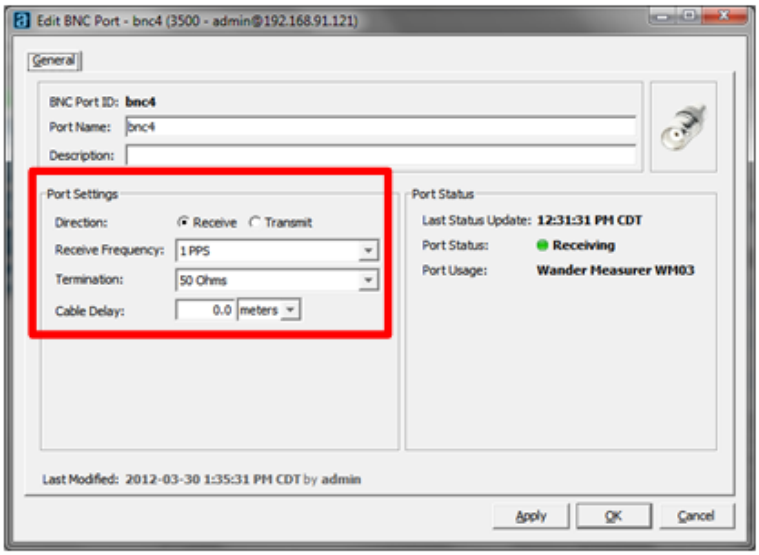
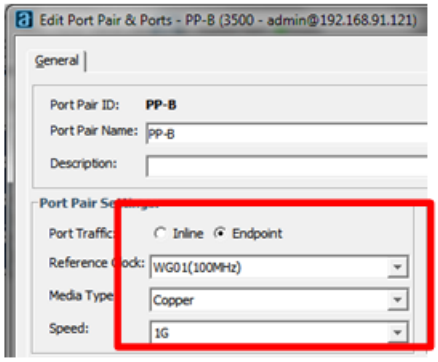


Figure 66. G.8261 / SyncE Test Setup

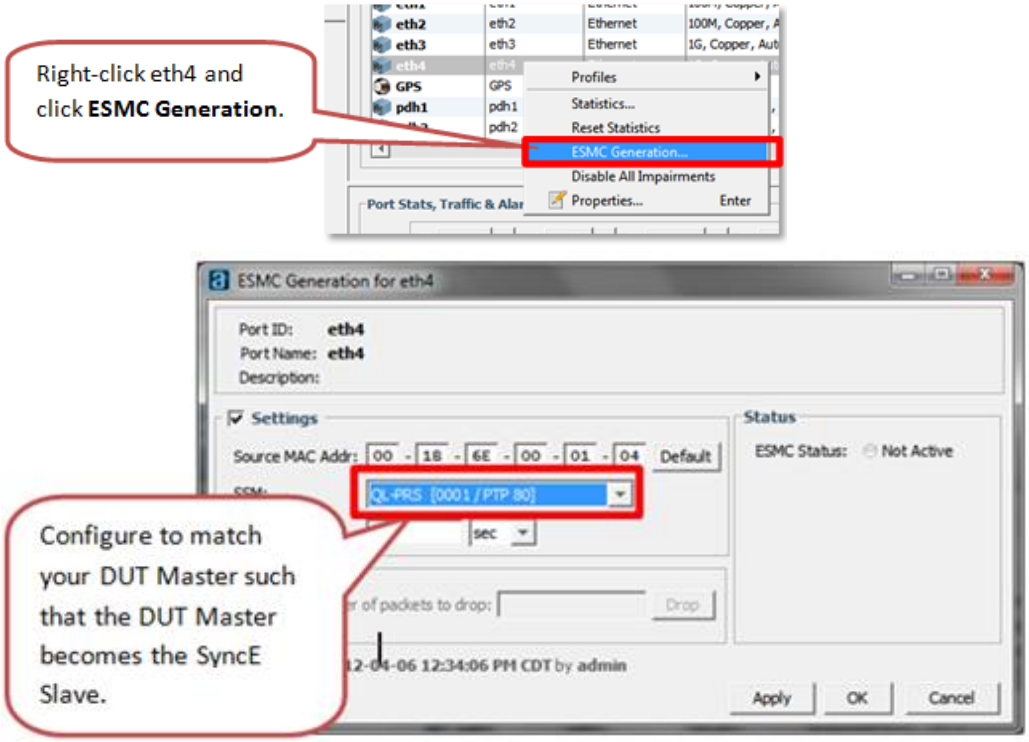
1. Connect the 3500 to the PTP/SyncE devices as shown in the diagram. Note that this testing requires two pairs of Ethernet ports. Eth4 from the 3500 should be connected to a SyncE slave port on the Master device to provide a frequency reference over SyncE.
2. Connect the 1PPS output from the Master and slave DUTs to BNC ports on the Anue 3500. Configure these BNC ports for Receive 1PPS, and configure the cable delay to match the length of cable connecting to each port.



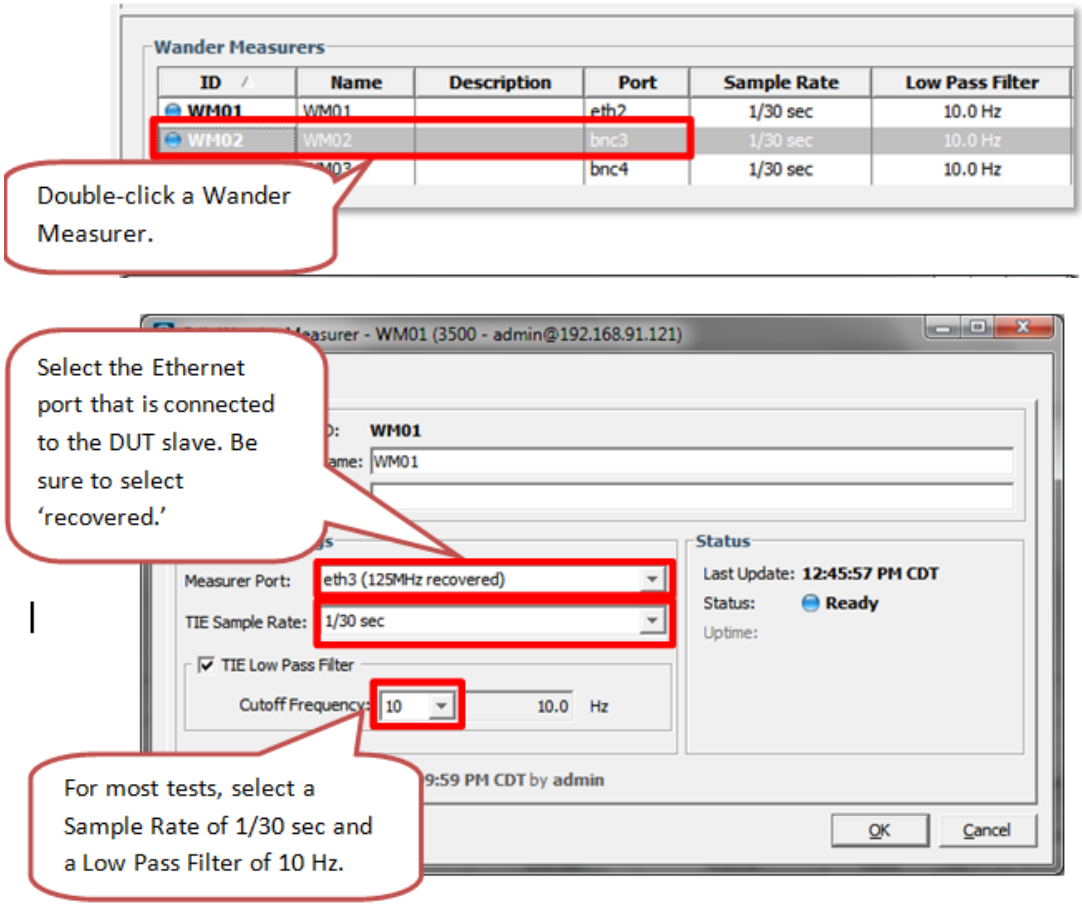
3. Port Pair PP-B is used to provide SyncE frequency reference to the Master device, and to measure the SyncE recovered clock on the slave.
    a. Set Port Pair PP-Bto **Endpoint** mode, and set the Reference Clock for WG01.



b. Configure ESMC Generation on Eth4 – configure to match the requirements of the DUT Master port connected to Eth4 for the DUT Master device to become slave.



c. Select a Wander Measurer from the Anue 3500 Control Panel's Wander tab to measure the DUT's Ethernet interface. Configure the Wander Measurer for the correct interface.



2. Port Pair A is used to apply packet-layer impairment (PDV) between the Master and Slave. Follow steps 6-7 from Setup in previous section *G.8261 Testing Timing Over Packet* to set up PDV Impairments.
3. With Synchronous Ethernet, the DUT Master and Slave should be synchronized in a matter of seconds.
4. Packet-layer impairment can be introduced on the PTP packet stream that is used to deliver time of day and phase. Configure PDV impairments as in Setup steps 6-7 of previous section *G.8261 Testing Timing Over Packet.*

Step-by-Step Instructions

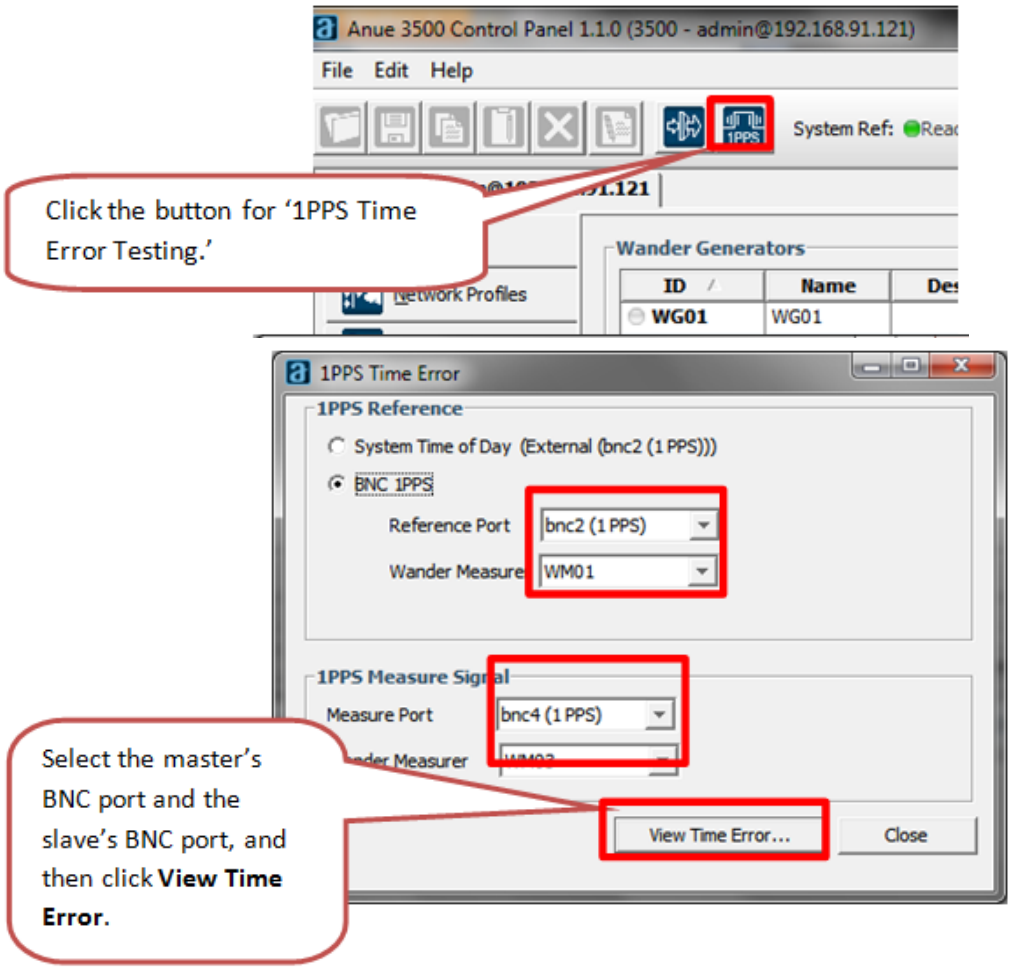
1. Once synchronization is complete, measure the Time of Day error in terms of phase (1PPS) from the Wander view of the 3500 Control Panel. See Results Analysis for details.

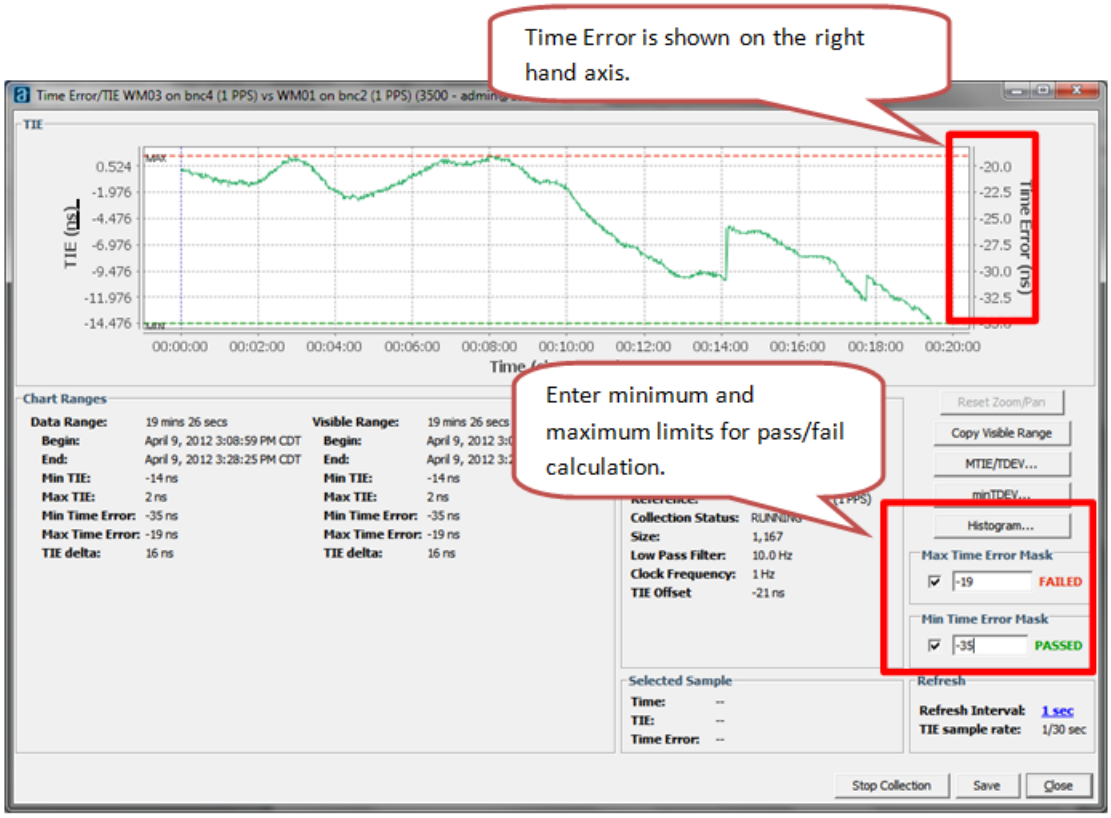
Test Variables

- Test with the system in both PTP **multicast** mode and in PTP **unicast** mode.
- Test with the system in both **one-step mode** (which reduces the number of messages) and in **two-step mode**.
- Test by using varying sync and follow-up packet rates or different PTP profiles as supported by the master and slave.
- Test multiple Ethernet speeds and on all supported interfaces (10G, 1G, and copper/optical).
- Test by using each of the G.8261 PDV test cases applicable to the equipment under test.

Results Analysis

1. To collect results, measure the Time of Day error in terms of phase (1PPS) from the Wander view of the 3500 Control Panel.





2. While testing Time Error on 1PPS, you can also measure MTIE and TDEV on the recovered clock interface on the slave, whether it is on BNC, PDH interface, or Ethernet. See previous test sections for details on configuring measurement of MTIE and TDEV on recovered clock interfaces.
3. While testing PTP and SyncE in hybrid mode, you can simultaneously introduce physical layer impairments on the Ethernet connection between the Master and Slave DUTs.

Conclusions

Next-Generation networks will require combination of SyncE and PTP to achieve the best synchronization of frequency and also accurate synchronization of time of day or phase. Testing SyncE and PTP in combination is therefore critical to ensure quality.

Contact Ixia

Corporate Headquarters
Ixia Worldwide Headquarters
26601 W. Agoura Rd.
Calabasas, CA 91302
USA
+1 877 FOR IXIA (877 367 4942)
+1 818 871 1800 (International)
(FAX) +1 818 871 1805
sales@ixiacom.com

Web site: www.ixiacom.com
General: info@ixiacom.com
Investor Relations: ir@ixiacom.com
Training: training@ixiacom.com
Support: support@ixiacom.com
+1 877 367 4942
+1 818 871 1800 Option 1 (outside USA)
online support form:
http://www.ixiacom.com/support/inquiry/

EMEA
Ixia Technologies Europe Limited
Clarion House, Norreys Drive
Maiden Head SL6 4FL
United Kingdom
+44 1628 408750
FAX +44 1628 639916
VAT No. GB502006125
salesemea@ixiacom.com

Renewals: renewals-emea@ixiacom.com
Support: support-emea@ixiacom.com
+44 1628 408750
online support form:
http://www.ixiacom.com/support/inquiry/?location=emea

Ixia Asia Pacific Headquarters
21 Serangoon North Avenue 5
#04-01
Singapore 5584864
+65.6332.0125
FAX +65.6332.0127
Support-Field-Asia-Pacific@ixiacom.com

Support: Support-Field-Asia-Pacific@ixiacom.com
+1 818 871 1800 (Option 1)
online support form:
http://www.ixiacom.com/support/inquiry/